Computation-Cost-Invariant Universal Space-Vector Pulse-width Modulation for Multilevel Inverters

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Abstract—This paper proposes a new universal space-vector pulse-width modulation (SVPWM) scheme with invariant computation cost for multilevel inverters. In the proposed SVPWM, the modulation triangle in Sector 1 is quickly identified in a 120° coordinate system transformed from the a-b coordinate system. Then, the switching states and duty cycles of the three vertices of the modulation triangle are determined by simple computations. The switching states in the other five sectors are obtained according to their simple relationships with those in Sector 1. The proposed SVPWM is independent of the voltage level of the inverter and does not require any prestored lookup table or iterative operation. Therefore, neither the execution time nor the memory usage of the proposed SVPWM increases as the inverter level increases. Moreover, the proposed SVPWM is universal and can be applied to any multilevel inverters with the PWM controls based on space vector diagrams. The proposed SVPWM is validated by hardware tests on a three-level, neutral-point-clamped inverter; its computation cost invariance is validated by implementations in a digital signal processor for three-phase inverters with voltage levels up to 201; and its superiority is demonstrated by a comprehensive comparison with existing SVPWM schemes.

Index Terms—Computation cost invariance, coordinate transformation, multilevel inverter, space vector pulse-width modulation (SVPWM), universal PWM.

I. INTRODUCTION

Multilevel inverters [1]–[7] have been widely used in industrial applications due to their distinct merits over the two-level inverters, such as stepped output waveforms with a lower harmonic distortion, reduced switch stress, lower instantaneous rate of voltage change dv/dt, and lower switching frequency. The control of multilevel inverters is commonly achieved by using a pulse-width modulation (PWM) technique. The PWM schemes for multilevel inverters mainly fall into two categories: carrier-based PWM (CBPWM) [8]–[13] and space-vector PWM (SVPWM) [14]–[28]. In a CBPWM, triangular carrier waves are usually generated and compared with modulation signals to generate PWM gate signals. The CBPWM has low computational complexity. However, the design of CBPWM is not universal and depends on the topology and level number of the inverter. To achieve the levels of performance metrics, such as DC-link voltage utilization and balance, inverter efficiency, common-mode voltage (CMV) reduction, etc., comparable to those of the SVPWM schemes, specific designs and additional measures are usually needed in the CBPWM schemes for multilevel inverters with different topologies and/or voltage levels. For example, an appropriate zero-sequence voltage signal is usually generated and injected into the sinusoidal reference voltage signals [9]–[13] to balance the DC-link capacitor voltages and/or eliminate/reduce the low-frequency oscillations of the neutral point (NP) voltages of three-phase, three-level, neutral-point-clamped (NPC) inverters. Nevertheless, the zero-sequence-voltage injection in a CBPWM scheme depends on the topology and voltage level of the inverter, and can be complicated as mentioned in [29].

The SVPWM [14]–[28] is attractive due to its flexibility in optimizing various performance objectives, such as DC-link voltage balance, switching loss reduction, CMV reduction, etc. through the optimal selection of the switching sequence. However, a SVPWM scheme usually requires identification of the modulation triangle in which the reference vector is located, determination of the switching states for the modulation triangle, and calculation of the duty cycle for each switching state. For a three-phase, n-level inverter, there are usually \(6(n-1)^2\) triangles and \(n^3\) switching states in its space vector diagram. Thus, the computation cost and complexity of SVPWM schemes may increase significantly as the voltage level of the inverter increases. For example, some of the SVPWM schemes need iterative calculations to identify the subhexagon corresponding to a two-level SVPWM in which the tip of the reference vector is located [14], decompose the space vector diagram of an n-level inverter into hexagons (i.e., space vector diagrams) of two-level inverters for modulation triangle identification and switching states calculation [15], determine a set of nested hexagons to calculate the remainder vector and switching states [16], obtain the switching states of the three basic vectors in a line-to-line voltage coordinates system [17], or determine a set of nested hexagons to detect the nearest three vectors [18]. The execution time of the iterative calculations usually increases as the voltage level of the inverter increases. Some of the SVPWM schemes need a lookup table to prestore switching states [19], [20] or the switching sequences of at least one sector [21] offline for online determination of the switching sequence. The SVPWM of [22] needs four lookup tables to store all optimal duty cycles and switching sequences at different power factor angles. The SVPWM of [23] needs to use a \(2(n-1) \times n\) matrix generated offline to calculate the switching states for an n-level inverter. The memory usage of the lookup tables and matrix increases as the voltage level of the inverter increases.
In the \(m\)-mode SVPWM of [20], a five-segment switching sequence is determined in each switching cycle based on the controllability of different \(m\)-modes analyzed offline, where mode means switching state. Compared to the traditional SVPWM schemes using seven-segment switching sequences, the switching frequency of the \(m\)-mode SVPWM is reduced by one-third. However, the complexity of the \(m\)-mode controllability increases significantly as the voltage level increases, which limits the application of the \(m\)-mode SVPWM only to low-level inverters. For inverters with different voltage levels, the simplified SVPWM of [24] needs different formulas for duty cycle computation. As reported by [24], both the execution time and memory usage of the simplified SVPWM increase as the voltage level of the inverter increases.

The execution time and memory usage of the SVPWM of [25] and [26] are independent of voltage levels of inverters. However, both SVPWM schemes need a lookup table to prestore trigonometric values for calculating duty cycles, use six different sets of formulas for reference vectors in the six different sectors, and need three different sets of formulas to calculate switching states. In the SVPWM of [27], the nearest three vectors are identified and the corresponding duty cycles are computed via matrix transformations in a 60° coordinate system. The SVPWM of [28] transforms the reference vector into the stationary \(\alpha-\beta\) coordinate system. The switching states and duty cycles are then calculated by six different sets of formulas for the reference vector in six different triangles that form three different zones. However, neither [27] nor [28] discussed how to determine the switching sequence to improve the PWM control performance, such as capacitor voltage balance and switching loss reduction. Besides, no experimental results are provided in [27] or [28] to verify the analysis.

This paper proposes a new universal SVPWM scheme that has an invariant computation cost measured by execution time and memory usage for multilevel inverters with any voltage levels. In the proposed SVPWM, the three vertices of the modulation triangle in which the tip of the reference vector in Sector 1 is located are quickly identified in a 120° coordinate system transformed from the \(\alpha-\beta\) coordinate system commonly used by SVPWM schemes. Then, the switching states and duty cycles of the three vertices of the identified modulation triangle are determined by simple computations. The switching states in the other five sectors are obtained according to their simple relationships with those in Sector 1 in the 120° coordinate system. In a switching period, any vertex of the modulation triangle can be used as a starting point to determine the switching sequence with flexibly adjustable duty cycle(s) for the redundant switching state(s). Neither the execution time nor the memory usage of the proposed SVPWM changes with the voltage level of the inverter. Moreover, the proposed SVPWM is universal and can be applied to any multilevel inverters with the PWM controls based on space vector diagrams.

The remainder of this paper is organized as follows. Section II presents the proposed SVPWM scheme. Section III validates the proposed SVPWM by experimental results on a three-level NPC inverter and shows the computation cost invariance of the proposed SVPWM implemented in a digital signal processor (DSP) for three-phase inverters with voltage levels up to 201. Section IV compares the proposed SVPWM with existing SVPWM schemes. Section V concludes the paper.

II. PROPOSED SVPWM SCHEME

For an \(n\)-level inverter, the reference vector \(V_{\text{ref}}\) can be represented by

\[
V_{\text{ref}} = V_{dc} \left( S_a + S_b \cdot e^{\frac{2\pi}{3}} + S_c \cdot e^{\frac{4\pi}{3}} \right)
\]

where \(V_{dc}\) is the voltage of the DC source in each module for cascaded multilevel inverters or the voltage across each capacitor connected in series between the DC terminals for non-cascaded multilevel inverters, such as NPC; \(S_a, S_b,\) and \(S_c\) are the switching states of the phases A, B, and C, respectively. The values of \(S_a, S_b,\) and \(S_c\) vary from 0 to \(n-1\). Then, the output voltages of the phases A, B, and C with respect to the NP for cascaded multilevel inverters or the negative DC terminal for non-cascaded multilevel inverters are \(S_aV_{dc}, S_bV_{dc},\) and \(S_cV_{dc},\) respectively.

The space vector diagram of a three-phase, \(n\)-level inverter is shown in Fig. 1. In the diagram, the three numbers at each vertex denote the switching state \(\{S_a, S_b, S_c\}\) of the inverter. There are totally \((3n^2 - 3n + 1)\) vertices and \(n^2\) switching states, among which \((n - 1)^2\) are redundant switching states for \((3n^2 - 9n + 7)\) vertices in the space vector diagram. Due to space limit, only the switching states of some vertices are given in Fig. 1 for illustration purpose. Some vertices have \(d (d > 1)\) switching states, among which \(d - 1\) are named redundant switching states. The whole process of the proposed SVPWM scheme is to identify the modulation triangle (e.g., \(P_1P_2P_3\)) which encloses the tip of the reference vector (e.g., \(V_{\text{ref}}\)) determine the nearest three vectors (e.g., \(OP_1, OP_2,\) and \(OP_3\)) based on the three vertices of the modulation triangle, determine the switching states for the three vertices of the modulation triangle, and finally calculate the duty cycles of the nearest three vectors identified to synthesize the reference vector.

A. Identification of Modulation Triangle and Nearest Three Vectors

The space vector diagram is divided into six sectors, as shown in Fig. 1. The angle of each sector is \(\pi/3\), starting from the A-axis. The length of each side of a small triangle (e.g., \(P_1P_2P_3\)) in the diagram is assumed to be unity.

For any given reference vector with an angle \(\theta (\theta \in [0, 2\pi])\),
the sector number \( S = 1, 2, \ldots, 6 \) can be determined by

\[
S = \lfloor \frac{3\theta}{\pi} \rfloor + 1
\]

where \( \lfloor 3\theta/\pi \rfloor \) means rounding down to the nearest integer of \( 3\theta/\pi \). Since the duty cycle calculations in any of the six sectors are the same, the operation of the proposed SVPWM scheme is analyzed in detail for the reference vector in Sector 1. If the reference vector locates in one of the other five sectors, it is first converted to an equivalent reference vector in Sector 1 with an angle \( \delta (\delta \in [0, \pi/3]) \) calculated by using \( \theta \) as follows.

\[
\delta = \theta - (S-1)\pi/3
\]

Figs. 2 and 3 show the space vector diagrams of Sector 1 in the \( \alpha-\beta \) and 120° coordinate systems, respectively. The \( \alpha-\beta \) coordinates \( (V_\alpha, V_\beta) \) of a space vector in Fig. 2 can be transformed to the 120° coordinates \( (V_x, V_y) \) of the space vector in Fig. 3 as follows.

\[
\begin{align*}
V_x &= V_\alpha + V_\beta / \sqrt{3} \\
V_y &= 2V_\beta / \sqrt{3}
\end{align*}
\]

Let

\[
\begin{align*}
l_1 &= \lfloor V_x \rfloor \\
l_2 &= \lfloor V_y \rfloor
\end{align*}
\]

where \( l_1 \) and \( l_2 \) are the nearest rounding-down integers of \( V_x \) and \( V_y \), respectively.

The tip \( P \) of the reference vector \( OP \) can locate in any of the small triangles in Sector 1, which is called the modulation triangle. Through the coordinate transform described by (4) and (5), one vertex, e.g., \( P_1 (l_1-l_2/2, \sqrt{3} l_2/2) \) with \( 1 \leq l_1 \leq n-2 \) and \( 0 \leq l_2 \leq n-2 \), of the modulation triangle enclosing the tip \( P \) of the reference vector \( OP \) in the \( \alpha-\beta \) coordinate system of Fig. 2 is quickly identified as the base point, e.g., \( P_1 (l_1, l_2) \), in the 120° coordinate system of Fig. 3. Then, the origin \( O \) of the reference vector \( OP \) is shifted to the identified base point. The duty cycles of the nearest three vectors, i.e., the vectors from the origin \( O \) to the three vertices of the modulation triangle, can be calculated in the same way as that for the two-level SVPWM scheme. This is explained in detail later.

By connecting the identified base point and the tip of the reference vector, the remainder vector, e.g., \( P_1 P \), is generated.

\[
P_1 P = OP_1 - OP
\]

The remainder vector is enclosed by the modulation triangle.

The base point is identified, additional effort is still needed to determine the modulation triangle because different reference vectors with the tips located in different small triangles may have the same base point. For example, according to (4) and (5), the two reference vectors with the respective tips at \( (l_1+1/2-l_2/2, \sqrt{3} l_2/2+1/2) \) and \( (l_1-l_2/2, \sqrt{3} l_2/2+1) \) in the \( \alpha-\beta \) coordinate system have the same base point \( (l_1, l_2) \) in the 120° coordinate system. However, the two tips locate in different small triangles \( P_1 P_3 P_4 \) and \( P_1 P_3 P_5 \), respectively. To address this issue, the modulation triangle (e.g., \( P_1 P_3 P_4 \) or \( P_1 P_3 P_2 \)) in which the remainder vector is located is further identified as follows:

1) If \( (V_x - V_y) \geq (l_1 - l_2) \), the remainder vector locates in the upward triangle I, as shown in Fig. 4(a), named type I modulation triangle, e.g., \( P_1 P_3 P_4 \) in Fig. 3.

2) If \( (V_x - V_y) < (l_1 - l_2) \), the remainder vector locates in the downward triangle II, as shown in Fig. 4(b), named type II modulation triangle, e.g., \( P_1 P_3 P_2 \) in Fig. 3.

After the modulation triangle is identified, the next step is to calculate the 120° coordinates of the other two vertices. For the type I modulation triangle, according to the base point \( (l_1, l_2) \) in Fig. 4(a), the coordinates of the other two vertices are \( (l_1+1, l_2+1) \) and \( (l_1+1, l_2) \), respectively. For the type II modulation triangle, according to the base point \( (l_1, l_2) \) in Fig. 4(b), the coordinates of the other two vertices are \( (l_1, l_2+1) \) and \( (l_1-1, l_2+1) \), respectively. The three vertices of the identified modulation triangle represent the tips of the nearest three vectors of the reference vector starting from the original \( O \) in the \( \alpha-\beta \) coordinate system. The nearest three vectors will be used to synthesize the reference vector for the PWM control.

The process of identifying the modulation triangle and its three vertices in the 120° coordinate system according to the reference vector in the \( \alpha-\beta \) coordinate system is independent of the voltage level \( n \) of the multilevel inverter. Therefore, the execution time and storage memory needed to determine the modulation triangle and its three vertices do not change with the voltage level of the inverter.

B. Determination of the Switching States of the Three Vertices of the Modulation Triangle in Sector 1

Let the integer \( m \) be the total number of the switching states of any vertex of the modulation triangle in Sector 1. The value of \( m \) can be determined according to the voltage level \( n \) of the inverter and the 120° coordinates \( (x, y) \) of the vertex as follows.

\[
m = n - x
\]

For any of the three vertices of the modulation triangle in
Sector I, the \(i\)th switching state \([S_a(i), S_b(i), S_c(i)] (i = 1, \cdots, m)\) of the phases A, B, and C of an \(n\)-level inverter can be determined using the following simple formula.

\[
\begin{align*}
S_a(i) &= x + i - 1 \\
S_b(i) &= y + i - 1 \\
S_c(i) &= i - 1
\end{align*}
\]  

(8)

For example, for the vertex \(P_1\) with the 120° coordinates \((l_1, l_2)\) in Fig. 3 and 4, the value of \(m = n - 1\). Thus, the switching states of \(P_1\) are \([l_1, l_2, 0], [l_1+1, l_2+1, 1], \cdots, [n-1, n-l_1-1, n-l_2-1]\).

In each switching period, only four switching states of the modulation triangle are required in the switching sequence and, therefore, need to be calculated using (8); all other unused switching states of each vertex of the modulation triangle do not need to be calculated. This indicates that the process of determining the switching states in each switching period is also independent of the voltage level \(n\) of the inverter.

C. Determination of the Switching States of the Vertices in Sectors 2-6

If the original reference vector locates in a sector other than Sector I, its switching states can be simply determined using Table I according to the switching states of the three vertices of the modulation triangle identified in Sector I, where Table I summarizes the switching state relationships between a vertex in Sector I and the corresponding vertices in the other five sectors. For example, if the switching state of a vertex \((2, 1)\) in Sector 1 is \([2, 1, 0]\), then, according to Table I, the switching states of the corresponding vertices in other five sectors are \([1, 2, 0], [0, 2, 1], [0, 1, 2], [1, 0, 2],\) and \([2, 0, 1]\), respectively.

D. Calculation of Duty Cycles for the Nearest Three Vectors

To synthesize the reference vector using the nearest three vectors identified, the duty cycles of their tip vertices need to be calculated. If the reference vector \(OP\) locates in the type I modulation triangle \(P_1P_5P_4\), the following equation can be obtained according to the voltage-second average law:

\[
OP \times T = OP_1 \times t_1 + (OP_1 + OP_2) \times t_2 + (OP_1 + OP_3) \times t_3
\]  

(9)

where \(T\) is the switching period; \(t_1, t_2\), and \(t_3\) are the duty cycles of the nearest three vectors \(OP_1, OP_2,\) and \(OP_3\). Rearranging (9) yields

\[
OP \times T = OP_1 \times t_1 + OP_2 \times t_2 + OP_3 \times t_3
\]  

(10)

According to (9) and (10), the vectors \(P_1P_5, P_1P_4,\) and \(P_1P_3\) in the type I modulation triangle \(P_1P_5P_4\) are equivalent to the original nearest three vectors \(OP_1, OP_2,\) and \(OP_3\) of the reference vector \(OP\), respectively. Finally, the duty cycles of \(OP_1, OP_2,\) and \(OP_3\) can be obtained from (10) as follows:

\[
\begin{align*}
t_1 &= (V_y - V_x + l_1 - l_2)T \\
t_2 &= (1 + l_2 - V_y')T \\
t_3 &= T - t_1 - t_2
\end{align*}
\]  

(11)

Since four switching states are selected for the three vertices of the modulation triangle in each switching period, one of the three vertices will use two switching states and can be selected as the start point of the switching sequence. The duty cycles \(t_{h1}\) and \(t_{h2}\) \((h = 0, 1, or 2)\) of the two switching states of the start vertex can be adjusted flexibly as follows.

\[
t_{h1} = (1 + v) t_h/2 \quad and \quad t_{h2} = (1 - v) t_h/2, \quad -1 \leq v \leq 1
\]  

(13)

where \(v\) is a distribution coefficient. Usually, the base point \((l_1, l_2)\) can be selected as the start vertex of the switching sequence.

As shown in (11) and (12), the process of calculating the duty cycles of the nearest three vectors only depends on the 120° coordinates of the reference vector \((V_x, V_y)\) and base point \((l_1, l_2)\) and, thus, is independent of the voltage level \(n\) of the inverter.

E. Flowchart and Highlight of the Proposed SVPWM Scheme

Fig. 5 shows the flowchart of the proposed SVPWM scheme, which only involves several simple calculations and none of the calculations depends on the voltage level \(n\) of the inverter. Moreover, none of the steps of the proposed SVPWM depends on the topology or application of the multilevel inverter. Thus, the proposed SVPWM is universally applicable to any multilevel inverter topologies and applications; and its computational complexity and implementation do not change with the voltage level or topology of the inverter.

III. VALIDATION RESULTS

The proposed SVPWM scheme is validated for the classical
### Table I

**Switching State Relationships Between Sector 1 and the Other Five Sectors**

<table>
<thead>
<tr>
<th>Sector</th>
<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$S_a$</td>
<td>$S_b$</td>
<td>$S_c$</td>
</tr>
<tr>
<td>2</td>
<td>$S_a - l_1$</td>
<td>$S_b + l_1 - l_2$</td>
<td>$S_c$</td>
</tr>
<tr>
<td>3</td>
<td>$S_a - l_1$</td>
<td>$S_b + l_1 - l_2$</td>
<td>$S_c - l_2$</td>
</tr>
<tr>
<td>4</td>
<td>$S_a - l_1$</td>
<td>$S_b + l_1 - 2l_2$</td>
<td>$S_c + l_1$</td>
</tr>
<tr>
<td>5</td>
<td>$S_a - l_1 + l_2$</td>
<td>$S_b - l_2$</td>
<td>$S_c + l_1 - l_2$</td>
</tr>
<tr>
<td>6</td>
<td>$S_a$</td>
<td>$S_b - l_2$</td>
<td>$S_c + l_1 - l_2$</td>
</tr>
</tbody>
</table>

---

**Fig. 5. Flowchart of the proposed SVPWM scheme.**

- Obtain the sector number $S$ and the angle $\delta$ in Sector 1:

  

  $S = \text{int}(3\theta / \pi) + 1$ and $\delta = \theta - (S - 1)\pi / 3$

- Determine switching states in Sector 1 (i.e., $S = 1$):

  

  \[
  \begin{aligned}
  S_a(t) &= l_1 + 1 - i \\
  S_b(t) &= l_2 + 1 - i, \quad i = (1, 2, \ldots, n - 1) \\
  S_c(t) &= l_1 - i \\
  \end{aligned}
  \]

- Determine switching states in Sector 2-6 from Table I:

- Type I modulation triangle:

  

  \[
  \begin{aligned}
  t_1 &= (V_{r'} - V_{r'} + l_1 - l_2)T \\
  t_2 &= (V_{r'} - l_1 - l_2)T \\
  t_3 &= T - t_2 - t_1 \\
  \end{aligned}
  \]

- Type II modulation triangle:

  

  \[
  \begin{aligned}
  t_1 &= (V_{r'} - V_{r'} + l_1 - l_2)T \\
  t_2 &= (V_{r'} - l_1 - l_2)T \\
  t_3 &= T - t_2 - t_1 \\
  \end{aligned}
  \]

- Determine duty cycles for the two switching states of the start and output duty cycles for all switching states to be used.

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The three-level NPC inverter [1] shown in Fig. 6 by experimental studies. Then, the computation cost invariance of the proposed SVPWM is verified by implementation in a TMS320F28335 DSP for multilevel inverters with the voltage level up to 201.

#### A. Application of the Proposed SVPWM to a Three-Phase, Three-Level NPC Inverter

A main concern over the use of NPC inverters is possible imbalance of DC-link capacitor voltages. Unbalanced DC-link capacitor voltages will increase voltage stress on devices and generate harmonics in the output voltage. It is well known that there are 19 space vectors and 27 switching states for the three-level NPC inverter [30]. The 19 space vectors can be classified into four categories based on their amplitudes, which are zero (e.g., $OO\_1$), small (e.g., $OP_i$), medium (e.g., $OP$), and large vectors (e.g., $OP_3$), as shown in Fig. 3 when $n = 3$, $l_1 = 1$, and $l_2 = 0$. According to the analysis in [30], the zero and large vectors do not affect the DC-link capacitor voltages; but the small and medium vectors affect the DC-link capacitor voltages because there are phases connected with the NP when they are used. Each of the six small vectors (e.g., $OP_1$) has two switching states (e.g., 100 and 211) that have an opposite effect on the DC-link capacitor voltages. Thus, when the DC-link capacitor voltages $V_{C1}$ and $V_{C2}$ are unbalanced, the relative durations of the two switching states of the corresponding small vector can be adjusted by the value of $n$ in (13) to balance the DC-link capacitor voltages.

For example, if the tip of the reference vector $V_{ref}$ is located in the type 1 modulation triangle $P_1P_2P_3$ (see Fig. 3) during a sampling period, the dwell times $t_{01}$ and $t_{02}$ of the two switching states 100 and 211, respectively, of the small vector $OP_1$ can be adjusted to balance the DC-link capacitor voltages. Specifically, if $V_{C1} > V_{C2}$, one phase should be clamped to the positive DC bus to discharge the upper DC-link capacitor in the switching cycle, which can be realized by setting $n = -1$ in (13) such that the entire dwell time $t_0$ is used by the switching state 211 (i.e., $t_{01} = 0$ and $t_{02} = 1$). Then, a seven-segment switching sequence 100($t_{01}/2) \rightarrow 200(t_{i1}/2) \rightarrow 211(t_{02}/2) \rightarrow 210(t_{i2}/2) \rightarrow 200(t_{i2}/2) \rightarrow 100(t_{01}/2)$ used by the SVPWM of [22] becomes a five-segment switching sequence 200($t_{i1}/2) \rightarrow 210(t_{i2}/2) \rightarrow 211(t_{02}/t_{01}+t_{02}/2) \rightarrow 200(t_{i2}/2) \rightarrow 210(t_{i2}/2) \rightarrow 200(t_{i2}/2) \rightarrow 100((t_{01}+t_{02})/2)$. Thus, phase C is clamped to the negative DC bus.

Compared to the seven-segment switching sequence used in [22], the number of switching transitions and, thus, the switching power loss of the five-segment switching sequence of the proposed SVPWM is reduced by 1/3, because there is no switching transition in one of the three phases clamped to a DC bus in a switching cycle. Moreover, the information of the three-phase load currents needed in the CGBPWM of [8] and [9] for balancing the DC-link capacitor voltages is no longer needed in the proposed SVPWM.

#### B. Experimental Results

A prototype (see Fig. 7) of the three-level NPC inverter in
Fig. 6 was constructed to validate the proposed SVPWM. The prototype used three insulated-gate bipolar transistor (IGBT) modules APTG1200TL60G-ND from Microsemi Corporation and a gate driver HCPL-316J. The parameters of the experiment setup are given in Table II. The prototype was tested with a star-connected, three-phase, resistive-inductive load. A programmable AC source (Chroma 61512) was used to provide the DC-link voltage. The voltages and currents in the system were measured by using voltage transducers LV20-P and current transducers CKSR 6-NP, respectively. The SVPWM was implemented in a TMS320F28335 DSP.

Fig. 8 shows the test results of the NPC inverter prototype controlled by the proposed SVPWM. During the test, a 4V DC offset is initially added to the measured value of the capacitor voltage $V_{C1}$ to generate imbalance between the two capacitor voltages $V_{C1}$ and $V_{C2}$. As a result, $V_{C1}$ has a 4V DC offset from its actual value while $V_{C2}$ has a 4V DC offset from its actual value; and the difference between $V_{C1}$ and $V_{C2}$ is around 8 V, as shown in Fig. 8(a). Then, from the middle of the horizontal time axis of Fig. 8(a) onwards, the measured values of $V_{C1}$ and $V_{C2}$ are used by the proposed SVPWM. As a consequence, the two unbalanced capacitor voltages become balanced in about 2 ms. The result shows the capability of the proposed SVPWM for balancing DC-link capacitor voltages. The line-to-line voltage $v_{ab}$ in Fig. 8(a) is slightly asymmetric in each fundamental period due to unbalanced capacitor voltages. The asymmetry is mitigated after the capacitor voltages become balanced. The load current amplitude is always around 12 A during the test.

Since the proposed SVPWM uses a five-segment switching sequence, the phase voltage $v_{ab}$ shown in Fig. 8(b) only has pulses in two-thirds the duration of each fundamental cycle. In contrast, if using the SVPWM of [22] with seven-segment switching sequence or the CBPWM of [8] and [31] with nine-segment switching sequence, the number of pulses of the phase voltage in each fundamental cycle will increase 50% or 100%, respectively, with respect to the proposed SVPWM. Thus, compared to the existing PWM schemes that use seven- or nine-segment switching sequence, the number of switching transitions in each fundamental cycle and, thus, the switching losses is reduced by 1/3 or 50%, respectively, when using the proposed SVPWM.

### C. Computation Cost Invariance

To verify the computation cost invariance of the proposed SVPWM, it was implemented in a TMS320F28335 DSP for a three-phase inverter with different voltage levels up to 201, where a digital to analog converter (DAC) AD5725 was used to generate the simulated voltage waveforms of the inverters. Fig. 9 shows the experimental waveforms of two-phase voltages and the corresponding line-to-line voltage of the 201-level inverter obtained from the DSP and DAC. The line-to-line voltage is a smooth sinusoidal waveform with a nearly zero total harmonic distortion without using any filter.

The execution time and memory usage of the proposed SVPWM tested for the 3-level NPC inverter in Section III.B as well as the 5-level and 201-level inverters in this subsection are always 2.8 μs and 4718 bytes, respectively. As explained in Section II, the whole process of the proposed SVPWM scheme, including modulation triangle identification, switching states determination, and calculation of the duty cycles of the three vertices of the modulation triangle, is independent of the topology and voltage level of the inverter, only requires simple algebraic calculations, and does not require any lookup table to store or iterative operations to calculate the switching states and the corresponding duty cycles. Thus, neither the execution time nor the memory usage of the proposed SVPWM changes with the voltage level or topology of the inverter.

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**TABLE II**

**PARAMETERS OF THE THREE-LEVEL NPC INVERTERPrototype**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-link capacitor $C_1$ and $C_2$</td>
<td>1000 μF</td>
</tr>
<tr>
<td>Load resistance per phase</td>
<td>4 Ω</td>
</tr>
<tr>
<td>Load inductance per phase</td>
<td>8.4 mH</td>
</tr>
<tr>
<td>DC-link voltage</td>
<td>120 V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>5 kHz</td>
</tr>
<tr>
<td>Base frequency</td>
<td>50 Hz</td>
</tr>
</tbody>
</table>

---

Fig. 7. Laboratory prototype of the three-level NPC inverter.

Fig. 8. Experimental results of the three-level NPC inverter prototype using the proposed SVPWM: (a) the line-to-line voltage $v_{ab}$, phase-A current $i_a$, and DC-link capacitor voltages $V_{C1}$ and $V_{C2}$; (b) the voltage $v_{ab}$.
Fig. 9. Experimental result of a 201-level inverter obtained from a DSP and DAC: two phase voltages and the corresponding line-to-line voltage.

IV. COMPARISON OF THE PROPOSED SVPWM AND EXISTING SVPWM SCHEMES

A comprehensive comparison of the proposed SVPWM and the existing SVPWM schemes of [14]-[28] is conducted and the result is provided in Table III. Firstly, iterative calculations are needed in the SVPWM of [14]-[16] for modulation triangle identification and in the SVPWM of [14]-[18] for switching states determination. The execution time of the iterative calculations increases as the voltage level of the inverter increases. Moreover, lookup tables are used in the SVPWM of [19]-[22] and a matrix needs to be stored in the SVPWM of [23] for switching states determination. The memory usage of the lookup tables and matrix increases as the voltage level of the inverter increases. Thus, the computation cost (i.e., execution time and/or memory usage) of the SVPWM [14]-[23] increases as the voltage level of the inverter increases. On the other hand, the SVPWM schemes [25]-[28] and the proposed SVPWM only use direct calculations to identify modulation triangle and determine switching states and, thus, have the computation cost invariant with the voltage level of the inverter. However, the algebraic operations of the direct calculations of the proposed SVPWM are less and/or simpler than those of the SVPWM [25]-[28] and, thus, have lower computation cost. For example, when implemented in the same DSP TMS320F28335, the execution time and memory usage of the SVPWM in [27] are 5.2 μs and 4721 bytes, respectively, for the inverter with the voltage level up to 201 tested in Section III.C, which are higher than 2.8 μs and 4718 bytes, respectively, of the proposed SVPWM. Although the SVPWM of [24] also uses direct calculations to identify modulation triangle and determine switching states, it needs different formulas to calculate duty cycles for inverters with different voltage levels. As a result, both the execution time and memory usage increase as the voltage level of the inverter increases, as reported by [24] itself.

By using five-segment switching sequence, as discussed in Section III.A, the proposed SVPWM can reduce the number of switching transitions and, thus, the switching losses of inverters by 1/3 or 50%, respectively, when compared to the PWM schemes using seven- or nine-segment switching sequence. This is shown by experimental results on a three-level NPC inverter in Section III.B. However, the issues of switching transitions and losses are not discussed in [14]-[16], [18], [19], [23]-[25], [27], [28]. The SVPWM schemes of [17], [20], [21], [26] discussed the use of five-segment switching sequences to reduce switching transitions and losses over seven-segment switching sequences. However, no experimental results are provided in [17], [21], [26] to verify the analysis. The SVPWM of [22] uses seven-segment switching sequence, which leads to 1/3 more switching transitions in each fundamental cycle and, thus, 1/3 more switching losses than the proposed SVPWM.

<table>
<thead>
<tr>
<th>SVPWM scheme</th>
<th>Modulation triangle identification</th>
<th>Switching states determination</th>
<th>Computation cost invariant</th>
<th>Switching transition/loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed</td>
<td>Direct calculation on reference voltage vector</td>
<td>Direct calculation by addition/subtraction only</td>
<td>Yes</td>
<td>Discussed</td>
</tr>
<tr>
<td>[14]</td>
<td>Iterative calculation</td>
<td>Iterative calculation</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[15]</td>
<td>Iterative calculation</td>
<td>Iterative calculation</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[16]</td>
<td>Iterative calculation</td>
<td>Iterative calculation</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[17]</td>
<td>Direct calculation on reference voltage vector</td>
<td>Iterative calculation</td>
<td>No</td>
<td>Discussed</td>
</tr>
<tr>
<td>[18]</td>
<td>Direct calculation on reference voltage vector; needs matrix operations</td>
<td>Iterative calculation</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[19]</td>
<td>Direct calculation on reference voltage vector</td>
<td>Lookup table</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[20]</td>
<td>Not needed</td>
<td>Lookup table</td>
<td>No</td>
<td>Discussed</td>
</tr>
<tr>
<td>[21]</td>
<td>Direct calculation on reference voltage vector; needs six different sets of formulas for six sectors</td>
<td>Lookup table</td>
<td>No</td>
<td>Discussed</td>
</tr>
<tr>
<td>[22]</td>
<td>Direct calculation on reference voltage and current vectors</td>
<td>Lookup table</td>
<td>No</td>
<td>Discussed</td>
</tr>
<tr>
<td>[23]</td>
<td>Not needed</td>
<td>Direct calculation by using a (2(n-1)\times n) matrix generated offline</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[24]</td>
<td>Direct calculation on reference voltage vector</td>
<td>Direct calculation by addition/subtraction and multiplication/division (duty cycles determination depends on voltage level of the inverter)</td>
<td>No</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[25]</td>
<td>Direct calculation on reference voltage vector</td>
<td>Direct calculation by addition/subtraction and min/max operations; six different sets of formulas for six sectors</td>
<td>Yes</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[26]</td>
<td>Direct calculation on reference voltage vector</td>
<td>Direct calculation by addition/subtraction and min/max operations; six different sets of formulas for six sectors</td>
<td>Yes</td>
<td>Discussed</td>
</tr>
<tr>
<td>[27]</td>
<td>Direct calculation on reference voltage vector; needs matrix operations</td>
<td>Direct calculation by addition/subtraction and min/max operations</td>
<td>Yes</td>
<td>Not discussed</td>
</tr>
<tr>
<td>[28]</td>
<td>Direct calculation on reference voltage vector</td>
<td>Direct calculation by addition/subtraction; six sets of formulas for three different zones</td>
<td>Yes</td>
<td>Not discussed</td>
</tr>
</tbody>
</table>

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The comprehensive comparison from the four aspects in Table III demonstrates the superiority of the proposed SVPWM over the existing SVPWM schemes.

V. CONCLUSIONS

This paper proposed a new universal SVPWM scheme having an invariant computation cost for multilevel inverters with any levels. In the proposed SVPWM, the modulation triangle in which the reference vector in Sector 1 is located was quickly identified in a 120° coordinate system, which was transformed from the α-β coordinate system. Then, the switching states and duty cycles of the nearest three vectors were determined by simple computations based on the modulation triangle identified, which does not require any lookup table or iterative computation. Thus, the proposed SVPWM is extremely computationally efficient. The switching states in the other five sectors were obtained according to their simple relationships with those in Sector 1, as shown in Table I. In addition, both the execution time and memory usage of the proposed SVPWM do not increase as the inverter level increases. Thus, the proposed SVPWM can be implemented in real time in a commercial low-cost DSP for inverters with any voltage levels. Finally, the proposed SVPWM is universal and can be applied to any multilevel inverter topologies as long as their PWM controls are based on space vector diagrams. The superiority of the proposed SVPWM over existing SVPWM schemes was discussed based on a comprehensive comparison.

REFERENCES