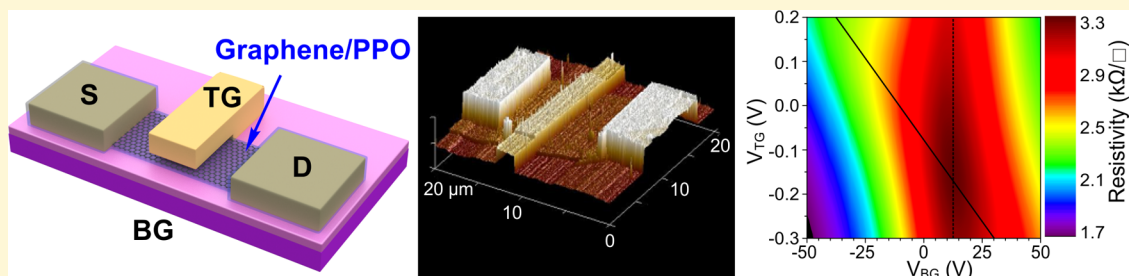


Electropolymerization of Poly(phenylene oxide) on Graphene as a Top-Gate Dielectric

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S Supporting Information



ABSTRACT: Site-directed electrochemical deposition of pinhole free, low- κ dielectric thin films on graphene is described for the first time. Specifically, we demonstrate the heterogeneous electrochemical polymerization of phenol to form thin (3–4 nm) layers of poly(phenylene oxide) (PPO) on monolayer graphene samples prepared by micromechanical exfoliation and chemical vapor deposition growth. We demonstrate the reliability of depositing PPO films simultaneously on a large number of devices, and selected individual graphene flakes/devices. The performance of top-gated field effect transistor devices described herein demonstrates the utility of electrodeposited PPO films as a top-gate dielectric.

INTRODUCTION

The high charge carrier mobilities exhibited by graphene have led to research efforts dedicated to the investigation of graphene-based field-effect transistors (FETs).^{1–3} Fabrication of a locally gated (top-gate) electrode on graphene to replace the traditional bottom-gated silicon would improve the applicability of graphene FETs operation at low power and high frequencies required for certain applications, including low noise amplifiers and electromechanical resonators.⁴ Ideal dielectric barriers separating the top-gate from the graphene need to be ultrathin (<10 nm), pinhole-free, and uniform. Construction of a top-gated electrode is difficult because of the incompatibilities of graphene with typical high dielectric constant (high- κ) barrier preparations. Pristine graphene has no functional groups, which hinders the modification of the surface with precursors commonly used for atomic layer deposition (ALD). The inability to modify the surface with precursors results in nonuniform films that nucleate primarily at the edges and defects of the graphene.⁵ Attempts to produce the desired dielectric film using techniques such as physical vapor deposition⁶ have resulted in the destruction of the graphene, while functionalization of the graphene with ozone^{7–9} and nitrous oxide¹⁰ result in nonuniform films or degraded carrier mobilities of the graphene FET.¹¹ One promising method to overcome the problems associated with coating graphene with high- κ dielectric materials is to incorporate a low dielectric constant (low- κ) polymer buffer layer or an organic seed layer. This low- κ dielectric layer on top

of graphene provides the functional groups necessary for the ALD precursors to adhere.^{12–15} Low- κ organics can also be used as tunnel barriers for bilayer pseudospin FETs^{16,17} and for tunnel spin injection.¹⁸ The organic dielectric films, which are required to be pinhole-free and uniform, have been previously fabricated by soaking the device in an adsorbate-containing solution,⁵ polymer spin coating,^{12,13,19} chemical vapor deposition,¹⁴ and gas-phase sublimation.¹⁵

Electropolymerization can be a useful tool for the preparation of organic films because of its experimental simplicity, because it is often performed at room temperature, and because film thickness can be controlled by controlling the charge passed and/or the potential at which the deposition is performed. Electropolymerization also provides some degree of dimensional specificity because film growth can be localized to the conductive substrates that are electronically attached to the potentiostat/galvanostat, leaving adjacent nonconductive materials uncovered by the film. Additionally, electrodeposited polymer films can conform to three-dimensional structures, including non-line-of-sight geometries.^{20,21} The thickness of electropolymerized insulating films is often self-limiting because the rate constant for polymerization rapidly decreases as the film thickness increases.

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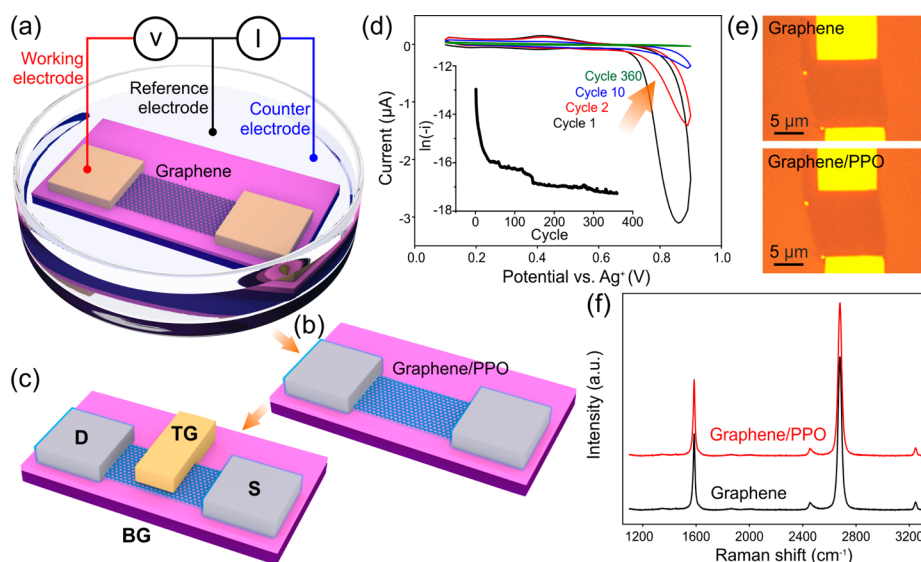


Figure 1. Fabrication of top-gated graphene FET with PPO dielectric. (a–c) Scheme of the device fabrication: (a) electropolymerization of phenol using a graphene FET as a working electrode results in (b) device covered with a thin PPO layer followed by (c) top gate (TG) fabrication over PPO in the last step. (d) Cyclic voltammetry (CV) of PPO deposition on a graphene device comparing the first (black), second (red), 10th (blue), and 360th (green) cycles in a phenol/ H_2SO_4 aqueous solution. Inset: The logarithm of the current at +0.9 V plotted vs the cycle number. (e) Optical microscopy images of a graphene FET before and after PPO deposition. (f) Raman spectroscopy of the same monolayer graphene before and after PPO deposition.

The electro-oxidation of phenol to poly(phenylene oxide) (PPO) can lead to particularly effective passivation of electrode surfaces. Rhodes et al.²² report that the conductivity and dielectric strength of PPO films prepared via electropolymerization are on the order of $7 \times 10^{-12} \text{ S/cm}$ and $1.7 \times 10^6 \text{ V/cm}$, respectively. Thin (<10 nm), pinhole free films of PPO can be formed using electropolymerization,^{22–25} and PPO is classified as a low- κ dielectric polymer for which the dielectric constant is reported to be as large as 2.98.^{24,26} With these precedents in mind, we endeavored to investigate the feasibility of electropolymerizing PPO onto graphene for subsequent use as a top-gate dielectric. A specific goal was to make the PPO films as thin as possible without introducing pinholes, with the ultimate expectation that high fields could then be generated across the dielectric without using large top-gate voltages.

EXPERIMENTAL SECTION

General Considerations. Phenol (Sigma-Aldrich, 99.5+%) and sulfuric acid (H_2SO_4 , EMD Chemicals, 95.0–98.0%) were used in the bath for electrodeposition of PPO. Silicon wafers with $300 \text{ nm} \pm 15 \text{ nm}$ of SiO_2 (Silicon Quest International) and graphite flakes (HOPG, Sigma-Aldrich) were used to prepare graphene flakes. PMMA950 A4 (4% poly(methyl methacrylate) in anisole, MicroChem Corp.), MMA EL6 (6% of the PMMA and ~8.5% methacrylic acid mixture in ethyl lactate, MicroChem Corp.), methyl isobutyl ketone:isopropanol (1:3) (MIBK:IPA, MicroChem Corp.), isopropanol (IPA, Sigma-Aldrich, 99.5+%), and acetone (Fisher Scientific, 99.7%) were used as received for electron beam lithography (EBL) patterning of electrodes onto graphene. Titanium (Ti, International Advanced Materials) and $1/4" \times 1/4"$ gold 99.999% (Au, International Advanced Materials) were evaporated by using an AJA E-beam apparatus.

Device Fabrication. Graphene Exfoliation. The well-known adhesive tape method was used to mechanically exfoliate graphene onto Si/SiO_2 substrate.²⁷ We searched for thin flakes using an optical microscope and then determined their thickness using Raman spectroscopy.

CVD Graphene Synthesis. Graphene films were grown by the chemical vapor deposition (CVD)²⁸ in a home-built CVD system. Twenty-five μm thick Cu foils (Alfa Aesar) were cleaned in acetic acid

for 10 min, then washed with water and IPA, dried and annealed in H_2 at 1000°C for 30 min. Methane was then introduced to the growth chamber, and graphene was grown at 1000°C for 15 min in a $\text{CH}_4:\text{H}_2$ (1:1) atmosphere at a total pressure of 550 mTorr. Upon removing the copper foil from the heating zone and quickly cooling it to room temperature, we then transferred the graphene to a clean Si/SiO_2 substrate using the wet transfer method described elsewhere.²⁹

Electrode Fabrication. MMA was spin-coated on the wafers at 3000 rpm for 45 s. The wafers were then placed on a hot plate at 180°C for 90 s and cooled for 1 min prior to adding a layer of PMMA by spin coating. The PMMA was also spin coated at 3000 rpm for 45 s. A Zeiss Supra 40 field-emission scanning electron microscope (SEM) and a Raith pattern generator were used to EBL pattern electrodes on the graphene. After being exposed, the wafers were developed in the MIBK mixture for 40 s, rinsed with 2-propanol, and dried with nitrogen gas. The AJA E-beam system was used to evaporate titanium at $0.1 \text{ \AA/s}$ until a thickness of 1 nm, as measured by a quartz crystal microbalance, was achieved. Ti evaporation was followed immediately by evaporation of 15 nm of gold at $0.1 \text{ \AA/s}$. The PMMA and excess metal were removed by liftoff for 30 min in acetone, rinsed with isopropanol and then water, and dried with nitrogen gas. Devices were then annealed for 10 min at 15 mTorr and 260°C to remove PMMA residues from the surface of graphene.

Poly(phenylene oxide) Deposition. An ultrasonic welder, West Bond 7476E manual wedge bonder, was used to make electrical contact between 0.0025 cm gold wires (Sempck) and the lithographically prepared Au/Ti contacts to the graphene. The source and drain electrodes were shorted during all electrodepositions to maintain the contacts and the graphene at the same nominal potential. A CHI 1200a potentiostat was used to control the potential of the graphene “working electrode” vs a silver pseudoreference electrode, which exhibited a potential of +0.070 V vs the saturated calomel electrode (SCE). A platinum wire was used as the counter electrode. A silicone gasket (Molecular Probes, P-18179, 1 mm thick) was placed on top of the wafer, exposing 1 mm in diameter of the graphene device. A reservoir was placed on top of the gasket and fastened with copper clips and screws. This cell setup is shown in the Supporting Information (Figure S1). Electrodeposition of PPO was accomplished by repeatedly cycling the potential into the oxidation wave for phenol in 50 mM aqueous solutions of phenol dissolved in 0.5 M H_2SO_4 .²³ After the deposition, the wafer was rinsed with water (18 Mohm cm)

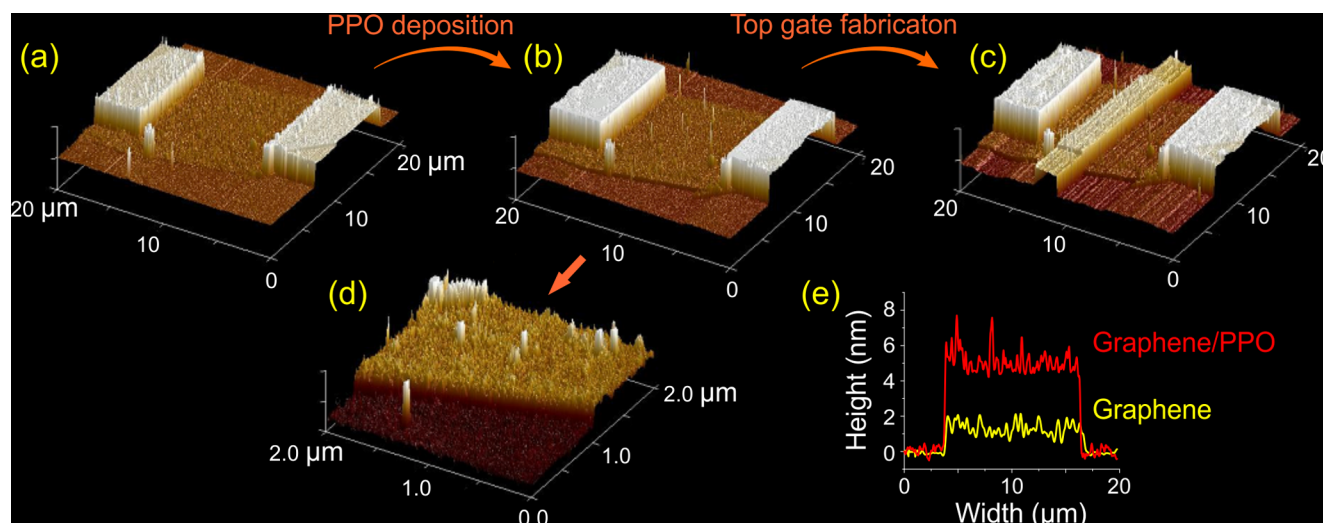


Figure 2. AFM images of a graphene FET device after (a) source/drain electrodes fabrication, (b) PPO electrodeposition, and (c) top gate fabrication. (d) Magnified AFM image of graphene edge after PPO electrodeposition. (e) Height profile of graphene before (yellow) and after (red) PPO deposition.

and dried under a stream of nitrogen. Graphene samples were annealed under vacuum (<20 mTorr) inside a glass tube (1 cm in diameter) inserted through the top of a Yamato Constant Temperature Oven DKN402. The samples were annealed at $150\text{ }^{\circ}\text{C}$ for 15 h after which time the tubes were removed from the oven and cooled to room temperature before exposing the sample to air.²²

Graphene Characterization. Atomic Force Microscopy (AFM). All AFM images were collected in air using a Dimension 3100 scanning probe microscope. The AFM was set to tapping mode using a silicon tip to measure thicknesses and roughness of the devices after each fabrication step. The AFM data were analyzed using NanoScope Analysis.

Raman Spectroscopy. Raman spectra were recorded at ambient conditions using a DXR Raman microscope with an excitation source of 10.0 mW at 532 nm .

Device Characterization. Current–Voltage Measurements. Field effect measurements were made using a model TTPX cryogenic probe station (Lake Shore Cryotronics). The samples were measured under a vacuum ranging from 2×10^{-6} to 8×10^{-6} Torr. Bottom-gated measurements were performed on the graphene FETs at various points during the fabrication process. All measurements were performed at room temperature. In all cases, the source–drain voltage (V_{DS}) was 0.1 V .

RESULTS AND DISCUSSION

Electropolymerization and Device Fabrication. Top-gated graphene FETs containing thin films of PPO as the dielectric layer were constructed in several steps. In short, a simple two terminal device on exfoliated graphene was patterned by means of electron beam lithography (EBL), and Ti/Au electrodes were deposited via electron beam evaporation (EBE). The PPO dielectric was then electropolymerized onto cleaned graphene that served as the working electrode in a three-electrode electrochemical cell (Figure 1a,b). Finally, EBL and EBE techniques were used to pattern a top electrode over the PPO (Figure 1c). See Experimental Section for details.

The electropolymerization of phenol to produce PPO on graphene was accomplished by continuously cycling the potential of the graphene working electrode between 0.1 and 0.9 V at a ramp rate of 100 mV/s (Figure 1d). Under these conditions a total of 360 cycles were typically completed to achieve the desired polymer thickness and uniformity. The black trace in Figure 1d shows the initial cycle in this set of 360

cycles. The peak at approximately 0.8 V is due to phenol oxidation, which leads to polymerization and passivation of the electrode. Subsequent cycles show the progressive decrease in the rate of polymerization due to the growth of a dense dielectric layer. Careful examination of the voltammograms shown in Figure 1d reveals that a rapidly diminishing reduction wave is also present at approximately 0.4 V for the first few cycles. We have not identified the process associated with this wave, but suggest that it is due to oxidized phenol (or short oligomers at or near the surface) that are not extensively coupled before potentials sufficient to reduce them are reached. It is noteworthy that Finklea et al. observe a similar wave under similar conditions.²³ The logarithmic inset in Figure 1d gives a better indicator of passivation process after the first cycles when the oxidative current falls to a small fraction of its original value. By the 360th cycle, the current falls to $<1\%$ of its initial value, leaving graphene with a uniform dielectric layer of PPO, which was then annealed in vacuum at $150\text{ }^{\circ}\text{C}$ for 15 h to remove remaining solvent and potentially improve stacking of the polymer chains.²²

PPO Film Characterization. Optical images of the same graphene device before and after PPO deposition (Figure 1e) suggest that electropolymerization is a mild process by which the mechanical integrity of graphene and its electrical contacts can be preserved at macroscales while maintaining surface cleanliness. Furthermore, Raman spectra of the same monolayer graphene flake before and after PPO deposition (Figure 1f) show no detectable damage to the graphene at nanoscales. The spectrum of graphene/PPO is similar to the original graphene flake, showing sharp G and 2D bands at 1586 and 2679 cm^{-1} respectively, with no detectable D band around 1340 cm^{-1} . The shape and position of the 2D band as well as the $\sim 1:2$ G-to-2D intensity ratio are all characteristic of a monolayer graphene.³⁰

Atomic force microscopy (AFM) was used to characterize the quality of the PPO films on the mesoscale. Figure 2 shows AFM images of a graphene FET after each fabrication step. Figure 2a, b shows the graphene, source (S), and drain (D) electrodes before and after being coated with the PPO dielectric. Figure 2c shows the same device after deposition of the top electrode. All three images have the same height

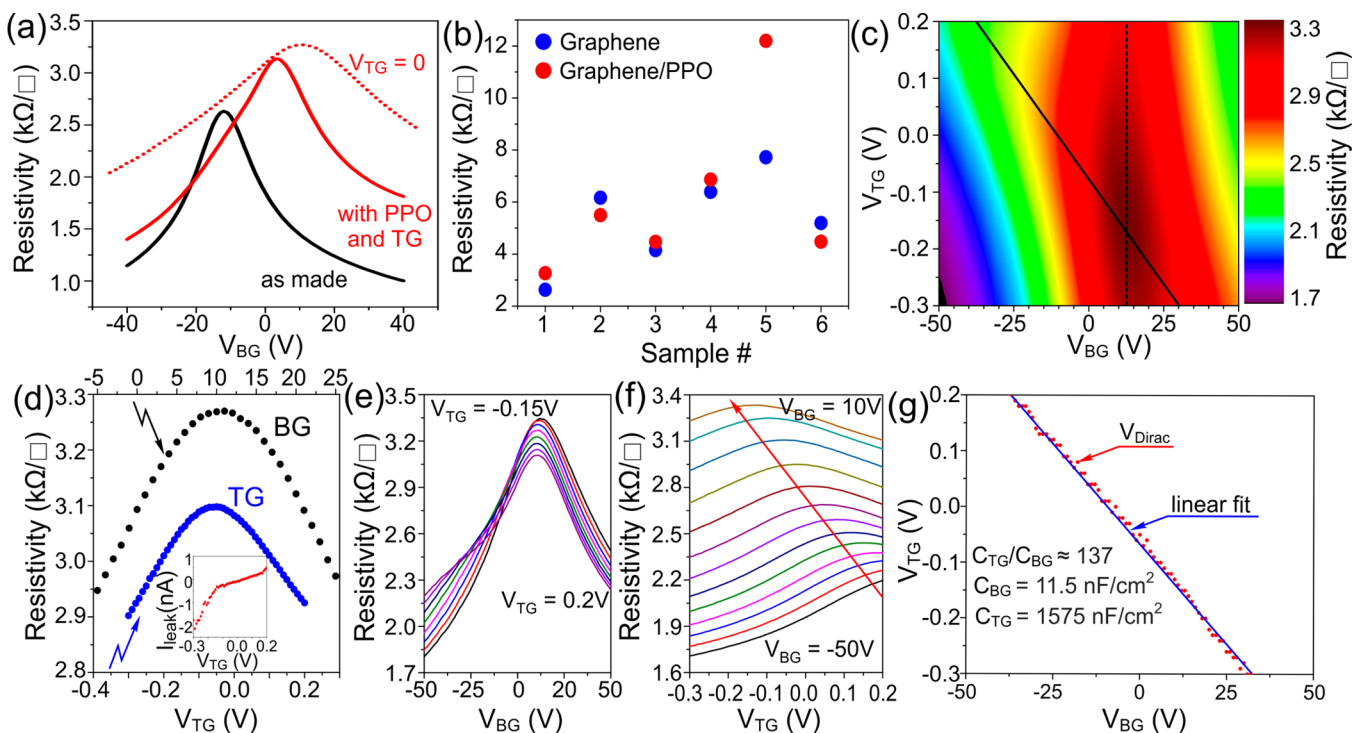


Figure 3. Electrical characterization of double-gated graphene FETs with PPO top-gate dielectric. All panels except for b show data for the same graphene FET that is shown in Figure 2c. (a) Graphene resistivity as a function of V_{BG} before (black) and after (both red lines) PPO deposition and top-gate electrode fabrication. Solid red and dashed red lines show ρ vs V_{BG} dependence when top-gate electrode is not grounded (floating voltage) and grounded ($V_{TG} = 0$), respectively. (b) Resistivity at V_{Dirac} for six graphene FETs before and after PPO deposition. (c) Resistivity of graphene FET with applied top and bottom gates. The black vertical (dashed) and black diagonal (solid) lines correspond to V_{Dirac} in nontop-gated and top-gated regions, respectively. (d) Comparison of resistivity plots for a double-gated graphene FET measured as a function of the V_{TG} with $V_{BG} = 0$ (blue) and measured as a function of the V_{BG} with $V_{TG} = 0$ (black). Inset: The leakage current between top-gate and source drain electrodes at different V_{TG} . (e) Dependences of graphene FET resistivity on the V_{BG} measured at different V_{TG} that varied from -0.15 to 0.2 V with the increment of 0.05 V. (f) Dependences of graphene FET resistivity on the top-gate voltages measured at different V_{BG} that varied from -50 to 10 V with the increment of 5 V. The red arrow illustrates the shift of the V_{Dirac} . (g) Dependence of V_{Dirac} on V_{TG} and V_{BG} . Red circles show experimental data points, whereas blue line represents the linear fit.

scale. Although the edge of graphene is barely visible on the scale selected for Figure 2a, this edge becomes readily apparent after the deposition of PPO, as shown in Figure 2b. The edge is prominent in Figure 2d, which is a section of Figure 2b displayed at more sensitive length scales. These images clearly show that PPO was selectively deposited on graphene/contacts and not over the entire substrate. Figure 2d and the representative height profiles shown in Figure 2e demonstrate that the PPO layer is free of pinholes on the mesoscale and that it is relatively smooth. To confirm the absence of pinholes in the PPO layer, we used a well-known electrochemical technique that measures possible permeation of small molecules through thin films.^{22,23} In our case we used cyclic voltammetry to monitor the reduction/oxidation of a small redox probe, $\text{Ru}(\text{NH}_3)_6^{3+}$, dissolved in solution. The detailed results of such measurements found in the Supporting Information demonstrate that the PPO films effectively block electron transfer between the probe and the underlying graphene electrode, allowing us to deduce that the films are free of pinholes on a length scale of a few Angstroms, the hydrated diameter of a $\text{Ru}(\text{NH}_3)_6^{3+/2+}$ cation.³¹

Additional comments concerning the height profiles in Figure 2 are warranted. In these particular profiles, the height of the graphene was measured to be 1.4 ± 0.4 nm relative to the wafer, and the height of the PPO coated graphene was measured to be 5.0 ± 0.6 nm relative to the wafer. Thus, we

estimate the PPO thickness to be 3.6 ± 0.7 nm. In both cases, the roughness measured for the wafer was approximately 0.2 nm. All uncertainties reported above are one standard deviation in the measured height. It should be noted that we were not able to measure these height profiles at exactly the same location on the device, before and after PPO polymerization. Although the PPO thicknesses were approximately 3.6 nm under these deposition conditions, our preliminary results, and the results of others, suggest that the thickness of the PPO can be controlled by controlling the deposition time through the number of cycles.³²

Electrical Measurements. To probe the electronic properties of double-gated graphene FETs with PPO top-gate dielectric, we fabricated five devices on mechanically exfoliated graphene flakes. Figure 3 shows the results of the electrical measurements for the FET shown in Figure 2c. Figure 3a illustrates the influence of PPO electrodeposition and top-gate fabrication on the resistivity (ρ) of graphene that was probed as a function of the bottom-gate voltage (V_{BG}). As made graphene device showed peak resistivity of $2.7 \text{ k}\Omega/\square$ at the Dirac point (V_{Dirac}), approximately -12 V. Graphene field-effect mobility (μ_{FE}) was estimated by selecting linear regime of the transport curve and fitting it with eq 1.³³

$$\mu_{FE} = \frac{1}{C_{BG}} \frac{d(1/\rho)}{dV_{BG}} \quad (1)$$

The resulting value, $\mu_{\text{FE}} = 1290 \text{ cm}^2/(\text{V s})$, is consistent with values found by others for graphene on SiO_2 .³⁴ After PPO electrodeposition and top-gate fabrication the resistivity increased slightly to $3.1 \text{ k}\Omega/\square$, and the V_{Dirac} shifted to approximately 4 V, indicating p-doping of graphene by PPO. Because of coupling between the top and bottom gates, charge carrier mobilities in double-gated devices are usually overestimated.^{35,36} To make a correct estimation of graphene mobility, we used ρ vs V_{BG} dependence when top-gate electrode was grounded (dashed red curve in Figure 3a). In this case the effective capacitance is equal to back-gate capacitance.³⁶ Again using eq 1, we estimate the mobility after top-gate electrode fabrication to be $335 \text{ cm}^2/(\text{V s})$. Data for mobility before and after PPO deposition for five additional devices are presented in Figure S4 in the Supporting Information. Overall, the change in mobility is moderate and consistent for all samples examined.

Figure 3b shows resistivities at V_{Dirac} for six graphene devices—one of which (sample 1) is depicted in Figure 2—before and after electrodeposition of the PPO top dielectric. Details for the five additional devices are presented in the Supporting Information (Figure S4). Resistivities for the uncoated graphene range from 2 to $7 \text{ k}\Omega/\square$, and with one exception (sample 5), little change in resistivity is observed upon deposition of the PPO. The total resistance for the devices consists of graphene resistance and contact resistance. The contact resistance was graphically determined to be $2.6 \pm 0.4 \text{ k}\Omega \mu\text{m}$ as presented in Figure S6 in the Supporting Information. Overall, the changes in resistivity show no systematic trend, and are consistent with the Raman spectroscopy, which indicates that the electropolymerization is a mild process.

Device performance as an FET is provided in Figure 3c, which is a resistivity map as a function of the top-gate voltage (V_{TG}) and V_{BG} . Resistivity vs V_{TG} dependence in 0.01 V increments was measured individually for each bottom gate voltage from -50 to 50 V in 1 V increments. The figure shows that the resistivity of a graphene FET can be independently tuned by either gate and the peak resistivity appears at approximately $V_{\text{BG}} = 12 \text{ V}$ and $V_{\text{TG}} = -0.15 \text{ V}$.

Several cross-sections of the resistivity map shown in Figure 3c are plotted in Figure 3d–f. Figure 3d shows the dependence of resistivity on gate voltage when voltage was applied to one gate (top or bottom) but the other was grounded (i.e., a cross-section at $V_{\text{TG}} = 0$ and $V_{\text{BG}} = 0$ respectively). This figure shows that the ambipolar field-effect behavior typical for graphene can be observed when either gate is applied. The leakage current through the top gate dielectric was 1.9 nA at $V_{\text{TG}} = -0.3 \text{ V}$ (Figure 3d, inset), indicating that the top gate does not penetrate through the PPO to the graphene.

Cross-sections of the resistivity map shown in Figure 3e and Figure 3f help to illustrate the shift of V_{Dirac} when voltage is applied to each gate electrode. Figure 3e shows the dependence of resistivity on V_{BG} when V_{TG} is varied from -0.15 to 0.2 V in 0.05 V increments. The shift of V_{Dirac} is negligible (also shown in Figure 3c as dashed line) and is due to the performance of the graphene device over areas not covered by the top-gate electrode.³⁷ Figure 3f shows the dependence of graphene resistivity on V_{TG} when V_{BG} is varied from -50 to 10 V in 5 V increments. In this case, V_{Dirac} clearly shifts toward more negative values when V_{TG} increases, as illustrated by the red arrow (Figure 3f) and marked by a solid black line in Figure 3c. This change is associated with the graphene area covered by the

top-gate electrode. Because the top-gate electrode covers only a small area of graphene device (see Figure 2c), the shift in V_{Dirac} is observed only when the dependence of graphene resistivity on V_{TG} is examined at various V_{BG} .

Figure 3f shows that for different values of V_{BG} the Dirac point is observed at different top-gate voltages. This dependence of V_{Dirac} on both top- and bottom-gate voltages is further illustrated in Figure 3g. For each experimentally selected V_{BG} , this Figure shows the corresponding V_{TG} at which the maximum resistivity is observed. V_{Dirac} corresponds to the charge neutrality point that is reached when a certain charge, q , is induced in graphene by applying either or both top- and bottom-gate voltages as described in eq 2

$$q = C_{\text{TG}}V_{\text{TG}} + C_{\text{BG}}V_{\text{BG}} \quad (2)$$

where C_{TG} and C_{BG} correspond to the top- and bottom-gate capacitances, respectively. The relationship between the two independent parameters, V_{TG} and V_{BG} (at V_{Dirac}) can be expressed by the algebraic rearrangement of eq 2 shown in eq 3.

$$V_{\text{TG}} = \frac{q}{C_{\text{TG}}} - \frac{C_{\text{BG}}}{C_{\text{TG}}}V_{\text{BG}} \quad (3)$$

This simple model is consistent with our experimental results, which show a linear relationship between V_{TG} and V_{BG} at V_{Dirac} .^{38,39} From the slope of a fit to these data, i.e., from the $C_{\text{BG}}/C_{\text{TG}}$ ratio, we estimate that $C_{\text{TG}} \approx 137C_{\text{BG}}$. The back-gate capacitance of this configuration is estimated to be $\sim 11.5 \text{ nF/cm}^2$, using a SiO_2 thickness of 300 nm and $k \approx 3.9$. Thus, we estimate the top-gate capacitance to be 1580 nF/cm^2 . Despite the low dielectric constant of PPO film, the capacitance per unit area is approximately three times larger than the one reported by Meric et al.⁴⁰ when using a high- k material, HfO_2 . In this case, for a 15 nm layer of HfO_2 and $k \approx 16$, C_{TG} was found to be 552 nF/cm^2 . The very large capacitance measured in our experiment is largely due to the small thickness of the PPO layer ($3.6 \pm 0.7 \text{ nm}$); however, it should be noted that use of a simple parallel plate model for the capacitance is problematic because it does not include the roughness of the PPO film, which is a significant fraction of its average thickness. Additionally, the dielectric constant of the PPO may be preparation dependent, and the effective distance between the top gate and the graphene might be smaller than the thickness of the PPO as measured by AFM (*vide supra*). Such a decrease in thickness could be in part due to the diffusion of metal atoms in the polymer during electron beam evaporation of the top gate.

Advantages of PPO Electrodeposition Method. A distinct attraction of the electropolymerization technique is the capability to selectively deposit a dielectric material only on the conductive materials connected to the potentiostat, i.e., the graphene and electrical contacts. If multiple graphene devices are present on a substrate, electrodeposition can be used to coat any specific surface or subset of surfaces that are electrically conductive. In many other deposition techniques the entire surface of substrate must be covered by dielectric material.^{6–11} To demonstrate the selectivity of the electropolymerization approach, we prepared a mechanically exfoliated graphene flake on Si/SiO_2 substrate (Figure 4a). Raman spectroscopy (Figure 4b) showed that the top right part of the graphene flake was a single layer. The flake was patterned into two isolated graphene patches using EBL. The contours of these patches are outlined in Figure 4a. An FET device was

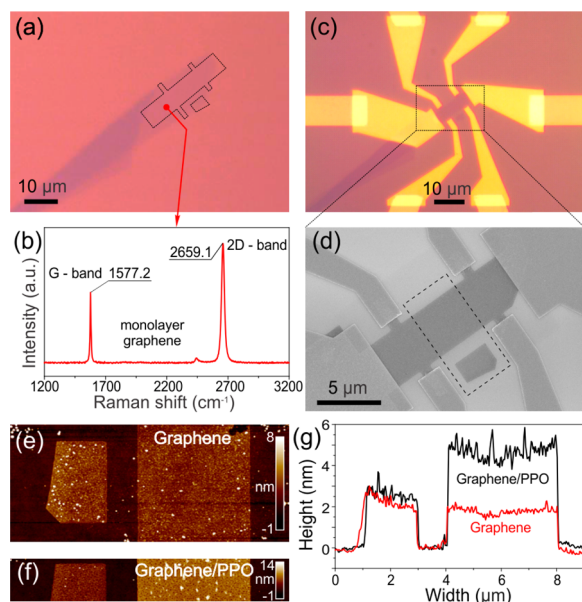


Figure 4. Selective electrodeposition of PPO on biased graphene. (a) Optical photograph of a graphene flake on Si/SiO₂ substrate. The dotted contours show two graphene patches that were later fabricated using EBL and dry etching. (b) Raman spectrum of the top right region of the graphene flake shown in a. (c) Optical image of an FET device fabricated from a larger graphene patch contoured in a. (d) SEM image of the same device. The dashed contour shows the area of the device channel and the isolated graphene patch characterized by AFM. (e, f) AFM images of the device channel and the isolated graphene patch (e) before and (f) after PPO electrodeposition. (g) Representative height profiles of materials shown in AFM images e and f.

then fabricated by EBL and EBE using a bigger graphene patch as a conductive channel bridging the Ti/Au electrodes. The smaller graphene patch remained electrically isolated from the larger one. Figure 4c shows an optical image of the device, and Figure 4d shows a SEM image of the device channel as well as the isolated graphene patch.

The PPO dielectric was electropolymerized onto the graphene device as described in the Experimental Section (Figure 1a). The graphene channel and the isolated graphene patch (the region outlined in Figure 4d) were imaged by AFM before and after PPO electropolymerization (Figure 4e, f, respectively). Figure 4g shows representative height profiles measured across the graphene channel and the isolated graphene patch. Before PPO electrodeposition, both graphene patches exhibit comparable heights, which was expected because they originated from the same monolayer graphene flake. The measured thickness for both graphene patches is ~ 2 nm, which is significantly larger than the interlayer distance in a graphite crystal (0.34 nm). However, prior to be characterized by AFM, the graphene flakes were subjected to EBL and dry etching. We attribute the increased thickness to residues of PMMA⁴¹ used as the etch mask, solvent molecules trapped underneath the graphene,⁴² and other adsorbates. Figure 4g shows that after PPO electropolymerization, the thickness of the graphene device channel serving as the working electrode increased by 3 nm. In contrast, the thickness of the isolated graphene patch, which was not biased during the electropolymerization, did not change. This result indicates that the deposition of PPO is spatially selective and occurs only on biased graphene. In summary, considerable care was taken to

ensure that the control (the unbiased graphene flake) was as similar as possible to the flake onto which the PPO was deposited. Both flakes originated from the same single layer of graphene, both were subjected to the same nanofabrication procedures, and both were exposed to the same electropolymerization bath for the same period of time. One was biased; one was not. These results demonstrate the present level at which we can spatially control the deposition of PPO.

Because of its high quality, mechanically exfoliated samples are typically used to characterize the intrinsic properties of graphene, but CVD-grown graphene is presently the material of choice for large-scale applications.⁴³ We have used CVD-grown graphene to provide additional evidence for the reliability and reproducibility of PPO electropolymerization on graphene. Furthermore, we show the feasibility of implementing the procedure to deposit the PPO dielectric on a large number of graphene FETs in a single step. Figure 5a shows the scheme of the device fabrication. First, large-scale monolayer graphene was grown by CVD on copper and transferred to a Si/SiO₂ substrate as described in the Experimental Section. The graphene thickness was confirmed by Raman spectroscopy (see Figure S7 in the Supporting Information). Using EBL and dry etching with PMMA serving as an etch mask material, we then patterned an array of eight graphene strips as schematized in Figure 5a(i). A second set of EBL and EBE steps were executed to fabricate Ti/Au electrodes, resulting in an array of eight graphene FETs, as depicted in Figure 5a(ii). All graphene devices in this array shared common contact (S), which is also served as the contact to the working electrode of a three-electrode potentiostat. The potentiostat was used to electrodeposit PPO on all eight graphene FETs in a single step (Figure 5a(iii)). Top-gate electrodes for all eight graphene FETs were then fabricated in a final set of EBL and EBE steps, as shown in Figure 5a(iv).

Figure 5b shows a photograph of the resulting array of double-gated graphene FETs with a common source (S) and bottom gate (BG), but separate drain (D) and top-gate (TG) electrodes. Figure 5c shows a photograph of one device in the array at higher magnification. AFM analysis shows that thin PPO layers were successfully deposited on all eight graphene channels. Representative AFM images of the same graphene FET channel before and after PPO electropolymerization are shown in Figure 5d, e, respectively. The AFM image of PPO-coated CVD graphene shows evidence of surface contamination, but this contamination is not due to the PPO electrodeposition. Features in similar locations with similar height profiles are observed in AFM images acquired before PPO deposition. It appears that this contamination occurred sometime during transfer of the CVD graphene from the copper foil to Si/SiO₂,⁴⁴ or that it is due to PMMA residues remaining from one or more of the lithographic steps.⁴¹ We observed these particulates in all AFM images of CVD graphene samples but not for mechanically exfoliated samples, suggesting more strongly that the presence of the particles occurs during CVD graphene transfer. Figure 5f shows representative height profiles measured across the graphene channel in Figure 5d, e, demonstrating that the thickness of the layer of electrodeposited PPO is ~ 5 nm. No discernible differences in average thickness were observed between different channels.

Figure 5g shows the influence of top and bottom gate voltages on resistivity for one of the devices in the array (Figure 5b); the curves were measured when only one gate voltage (top

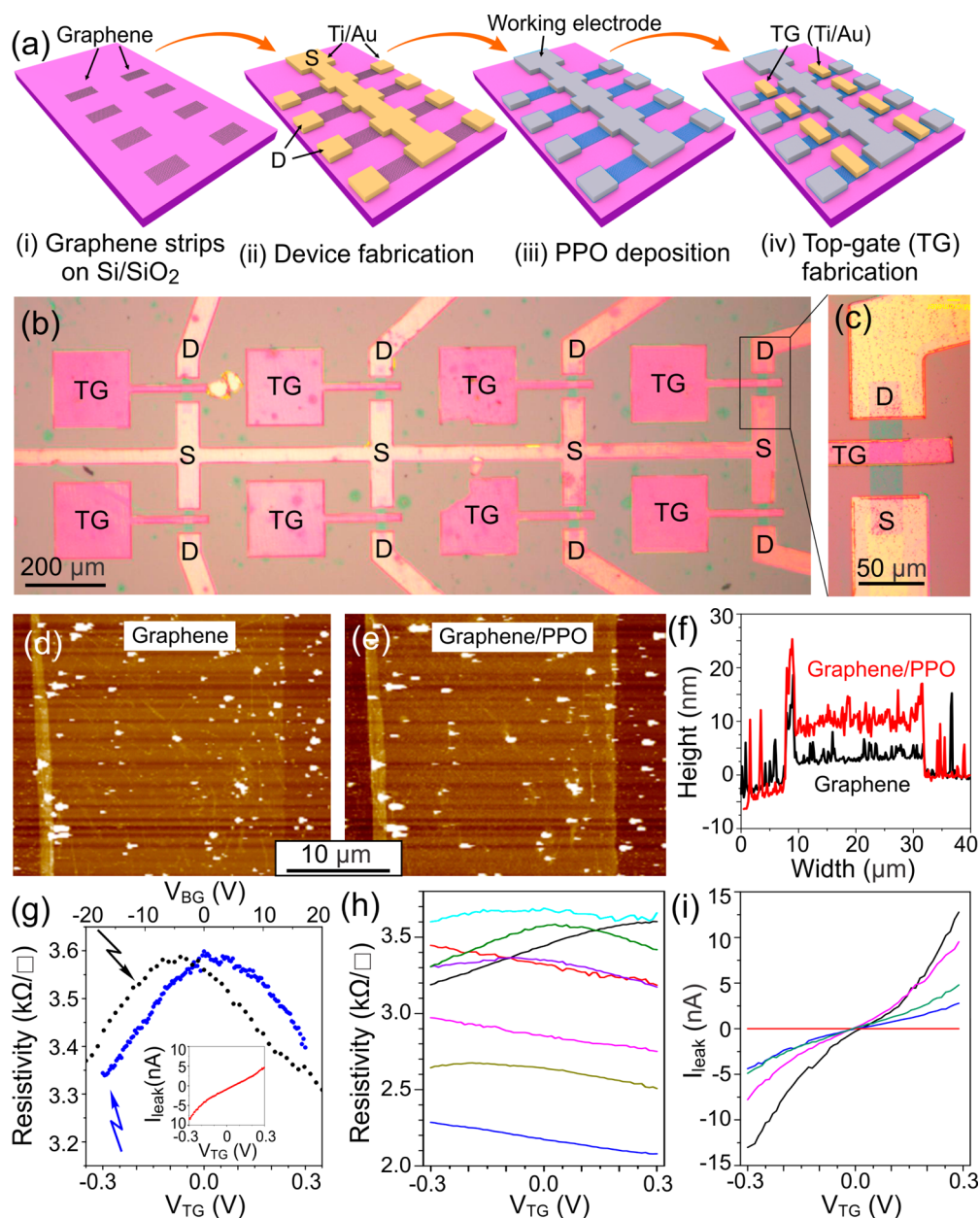


Figure 5. Array of double-gated FETs based on CVD-grown graphene with PPO top-gate dielectric. (a) Scheme of the fabrication of an array of double-gated graphene FETs. (b, c) Optical photographs of (b) the graphene FET array and (c) one of the devices in the array. (d, e) AFM images of the graphene device channel (d) before and (e) after PPO electrodeposition. (f) Representative height profiles for the AFM images shown in d and e. (g) Comparison of resistivity plots for a double-gated graphene FET measured as a function of the V_{TG} with $V_{BG} = 0$ (blue) and measured as a function of the V_{BG} with $V_{TG} = 0$ (black). Inset: The leakage current between top-gate and source drain electrodes at different V_{TG} . (h) Graphene resistivity as a function of V_{TG} for eight graphene FETs shown in (b). (i) Dependences of the top-gate leakage current on V_{TG} for five double-gated graphene FETs in the array.

or bottom) was applied. Similar to Figure 3d for devices based on mechanically exfoliated graphene, this figure shows that the ambipolar field-effect behavior is observed for the double-gated FETs based on CVD-grown graphene when either gate voltage is applied.

To demonstrate the reliability and reproducibility of the top-gate fabrication using electrodeposited PPO as the gate dielectric material, we compare the dependence of resistivity on V_{TG} for all eight graphene FETs in the array (Figure 5h). Each device was gated using an individual top gate electrode. The position of the Dirac point varies from device to device, which we attribute to subtle differences in the properties of the

CVD-grown graphene. Similar variabilities have been attributed to differences in defect concentrations, which manifest themselves in changed relative intensities of the G, D, and 2D Raman bands.²⁹

The quality of the electrodeposited PPO films was assessed by measuring the dependence of the leakage current on V_{TG} for all graphene FETs in the array. All devices showed a qualitatively similar dependence of the leakage current on V_{TG} , (see Figure 5i where five curves are shown), but the absolute values of the leakage current varied over several orders of magnitude. One of the graphene devices in the array exhibited exceptional dielectric properties showing a leakage

current of only $\sim 1 \times 10^{-12}$ amps across the PPO at $V_g = 300$ mV (see the red curve in Figure S1). Four devices shown exhibited a higher leakage current of $\sim 1 \times 10^{-8}$ A at $V_g = 300$ mV, and three other devices (not shown) passed $\sim 1 \times 10^{-7}$ A at $V_g = 300$ mV. Our results show that low leakage currents can be obtained for double-gated FETs constructed on mechanically exfoliated graphene and on CVD-grown graphene, demonstrating the utility of the PPO electropolymerization technique for introducing the top dielectric. Recent advances in cleaner transfer of CVD graphene from copper substrates⁴⁵ should help to decrease the leakage currents in arrays of double-gated graphene FETs containing electrodeposited PPO as the top-gate dielectric.

Finally, early in our attempts at preparing PPO dielectrics on graphene, we had some concern that the positive potentials necessary to oxidatively polymerize phenol might have a deleterious impact on the integrity of the graphene. Although Cordero⁴⁶ provides DFT calculations that show the electronic transfer from graphene to H_2SO_4 causes no change in graphene's semimetallic character, single-walled carbon nanotubes can be oxidized in concentrated sulfuric acid to form C–O bonds.⁴⁷ Furthermore, others have shown that irreversible oxidative degradation of graphite occurs at highly positive potentials in sulfuric acid.^{48,49} We have observed degradation of graphene at potentials positive of the onset of phenol oxidation in sulfuric acid. If the potential is cycled to +1.1 V instead of the usual +0.9 V required to polymerize phenol, pores develop in the graphene. When phenol is also present in the bath, the polymerization competes with pore formation, but the passivation does not dominate until pores grow to sizes that can be as large as 100 nm in diameter (see Figure S8 in the Supporting Information). We are currently investigating the possibility of using this process to control pore size and pore density in graphene thus forming graphene nanomeshes with a tunable electronic band gap.^{50,51}

CONCLUSIONS

Although we successfully demonstrate the electropolymerization of phenol to produce effective dielectric barriers on graphene, it is likely that this process can be further optimized. A large number of factors are expected to influence the properties of the polymer dielectric, including the rate at which the polymer is electrodeposited, the monomer concentration in solution, the solution pH, and the identity of the solvent. The dielectric efficacy of other organic thin films prepared by electropolymerizing monomers such as 4-chlorophenol,⁵² 2,6-dimethylphenol,⁵³ and *o*-phenylenediamine^{54,55} can also be investigated. Further improvement of the device fabrication includes using electrodeposited low- κ dielectrics as the seed layer on graphene for depositing high- κ dielectrics by ALD. Finally, by replacing the metal top-gate, the source, and the drain with conducting polymers such as poly(3,4-ethylenedioxythiophene) (PEDOT) that can be spin-coated, one might more readily imagine plausible pathways toward the construction of “all organic” flexible electronic devices.

ASSOCIATED CONTENT

Supporting Information

Additional figures and description of the device fabrication procedure and electrochemical cell design. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Notes

The authors declare the following competing financial interest(s): A full patent application has been filed.

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