The gate modulation of channel conductance of MoS_2 field effect transistor using 2D ferroelectric $CuInP_2S_6$

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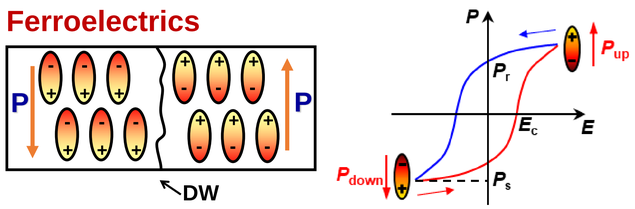
Abstract

This study examined the gating effect of two dimensional (2D) van der Waals (vdW) ferroelectrics $CuInP_2S_6$ (CIPS) in modulation of channel current of 2D semiconductor MoS_2 field effect transistor (FET). Recently, ferroelectricity has been discovered in 2D vdW materials, such as SnTe, In_2Se_3, and CIPS. These materials can potentially preserve ferroelectricity in the monoatomic layer limit, making them promising for developing ferroelectric-based 2D nanoelectronics.

In this study, we explored the gating effect on 2D MoS_2 FET top gated by 2D vdW ferroelectrics CIPS. The polarizations of CIPS on different base layers are robust after domain writing using conductive atomic force microscopy (AFM). The channel conductance has been sufficiently suppressed after transferring the CIPS top gate on MoS_2, which is due to the charge carrier depletion induced by the polarization of as-grown CIPS. We also use piezoresponse force microscopy (PFM) to switch the polarization of the CIPS top gate into the P_{up} and P_{down} states, which can induce non-volatile modulation of channel current and achieve a very large current on/off ratio of around 10^7. Our research can provide important material parameters for designing CIPS-based nanoelectronic devices, paving the path for their implementation in programmable, flexible nonvolatile memory, neuromorphic computing, and optoelectronic applications.

Introduction

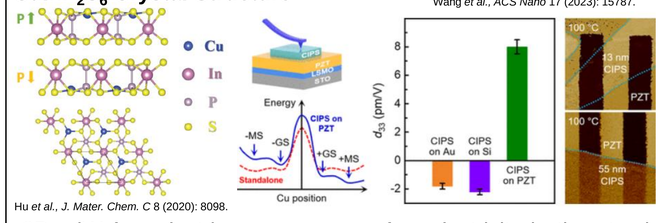
Ferroelectrics



- Ferroelectric shows the piezoelectric response under external electric fields
- Non-volatile polarization and switchable hysteresis

2D van der Waals (vdW) Ferroelectrics

$CuInP_2S_6$ Crystal Structure



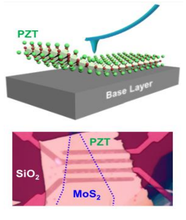
Hu *et al.*, *J. Mater. Chem. C* 8 (2020): 8098.

Wang *et al.*, *ACS Nano* 17 (2023): 15787.

- 2D vdW ferroelectrics can preserve ferroelectricity in the atomic layer limit, which is compromised for conventional ferroelectrics

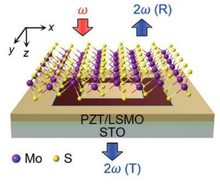
Application

Field Effect Transistor



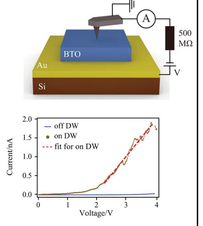
Wu *et al.*, *ACS Nanosci. Au* 3 (2023): 482.

Reconfigurable Optical Filters



Li *et al.*, *Adv. Mater.* 35 (2023): 2208825.

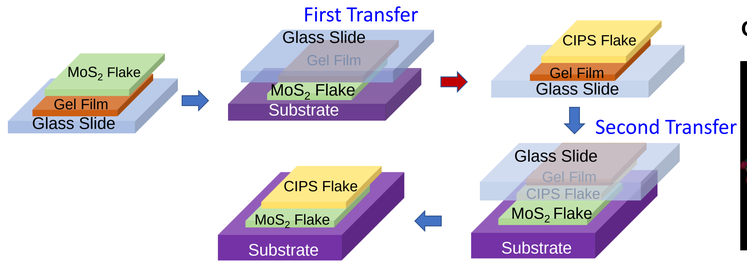
DW Memories



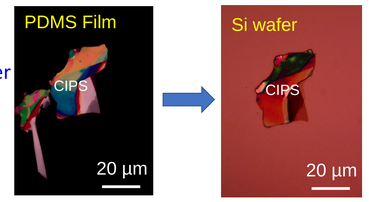
Sun *et al.*, *Nat Commun* 13 (2022): 4332.

Methods

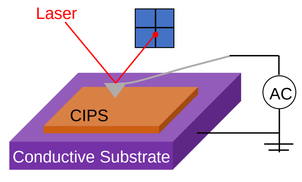
Transfer: CIPS Flake onto MoS_2 Flake

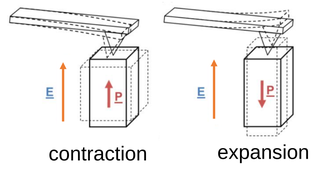


Optical images of CIPS

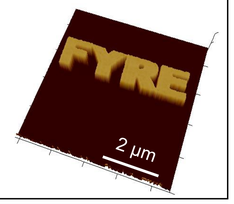


Characterization via Piezoresponse Force Microscopy



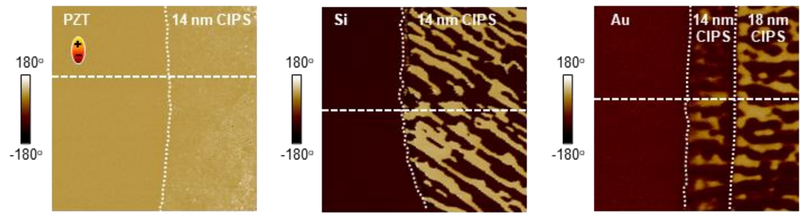


- Program polar patterns in ferroelectric thin films



PFM Imaging of CIPS flakes on different base layers

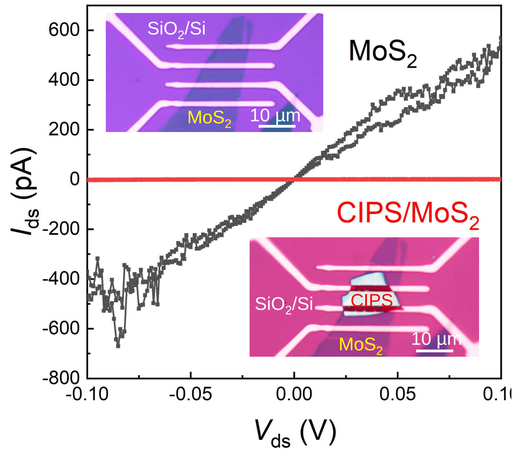
➢ **PFM Phase**



- ➢ CIPS on Si and Au: Spontaneous polarization formation of stripe domains
- ➢ Thin CIPS on PZT: Enhanced polar alignment

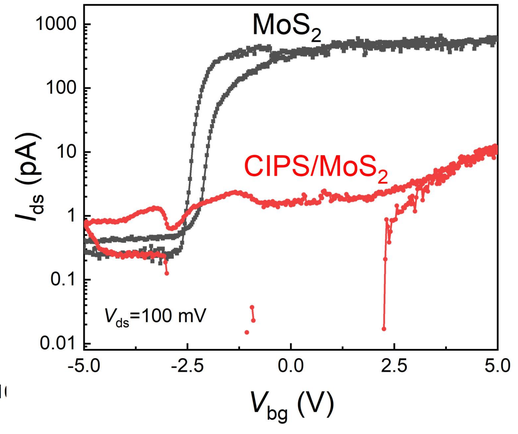
CIPS Top-gated MoS_2 FET

I-V characteristics



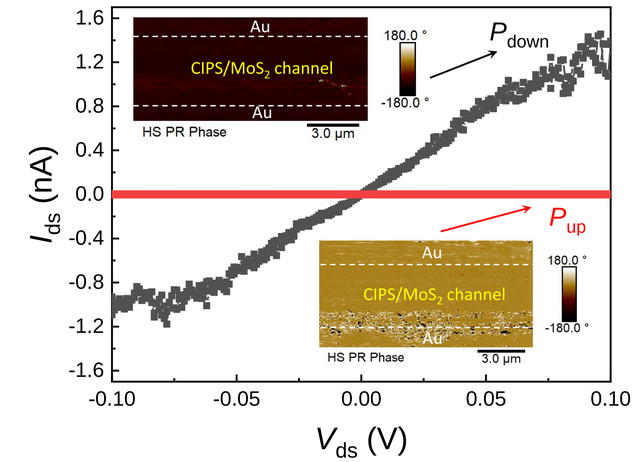
➢ I_{ds} is suppressed by over 3 orders of magnitude after transferring CIPS top gate

Transfer curves

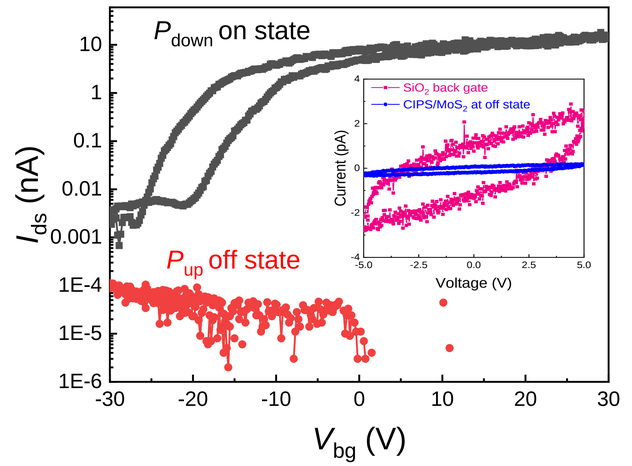


➢ The transfer curve shifts to the lower right-hand side after transferring CIPS

Gate modulation of CIPS/MoS_2 FET



- ➢ I_{ds} is suppressed by ~ 5 orders of magnitude after polarizing the CIPS top gate from P_{down} into P_{up} state
- ➢ The decreased channel current is due to the depressed charge carrier density induced by polarization of CIPS



- ➢ Large current on/off ratio of ~ 10^7 for P_{up} and P_{down}
- ➢ The CIPS/MoS_2 device at off-state is more insulating than SiO_2 back gate

Conclusion

- ➢ The domain of 2D ferroelectrics CIPS on Au and Si is stripe shape and the polar alignment is greatly enhanced when transferred on PZT base layer.
- ➢ The channel current of MoS_2 FET is greatly suppressed after transferring CIPS top gate.
- ➢ We could polarize the CIPS top gate into P_{up} and P_{down} states to induce the non-volatile modulation of channel current with a large on/off ratio of ~ 10^7.

Acknowledgements

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