Material for Room Temperature Single Electron Devices with Tunable Band Gap

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Abstract

Coulomb blockade due to local single-electron charging in granular nanomaterials leads to a conductance band gap at cryogenic temperatures. Recently, a conductance band gap behavior at room temperature was reported in a monolayer network array of one-dimensional necklaces of 10 nm Au particles. By controlling the size of the array from the microns to the submicron level, the band gap is linearly tuned over a remarkably large range, from 0.5 V to 7.5 V at 296 K, in this study. The linear behavior is explained in terms of a simple impedance-network model. The array size is controlled by a novel method using a combination of soft lithography and e-beam writing. The linear dependence of the threshold bias on array dimensions indicates that the transport is via a series of multiple individual tunnel junctions rather than variable range hopping or cotunneling. The threshold bias of over 2.5 V with a barrier energy of over 100 kT will potentially pave the way for building robust single-electron, device-based sensors operating at room temperature.

Background

- The band gap in electrical conductance of a material is a fundamental characteristic required for the rational design of electronic devices.
- A band-gap-like effect in nanoparticles and their array is caused by local charging at a single-electron level usually at cryogenic temperatures
- Single electron devices are switching type devices that operates at high speed with low power consumption.
- Unfortunately, above cryogenic temperatures, the band gap of the nanoparticle's array vanishes.
- However, in an array with local or global one-dimensional (1D) nanoparticle necklace characteristics, the effect of temperature (T) on the threshold bias (V_T) is significantly diminished (nominally independent of T) and a V_T as high as ~1 V is obtained at room temperature.

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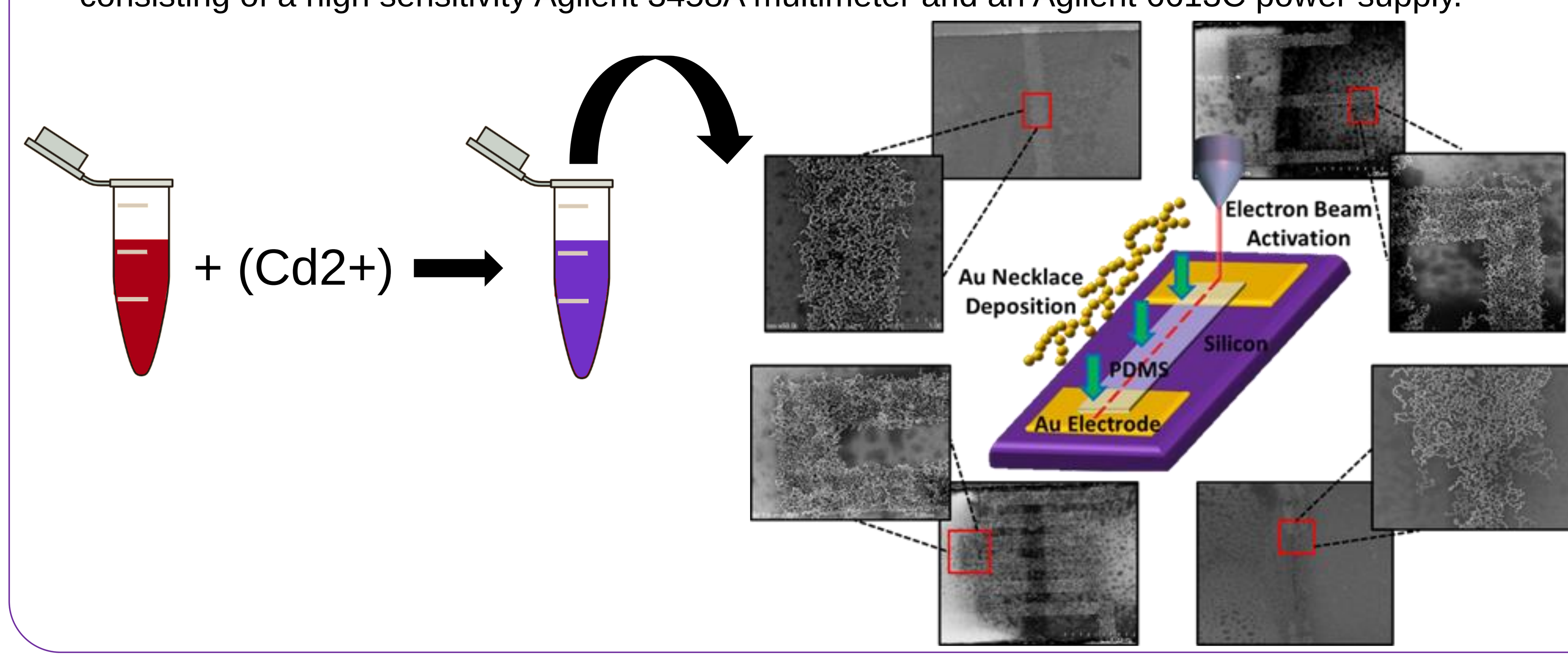
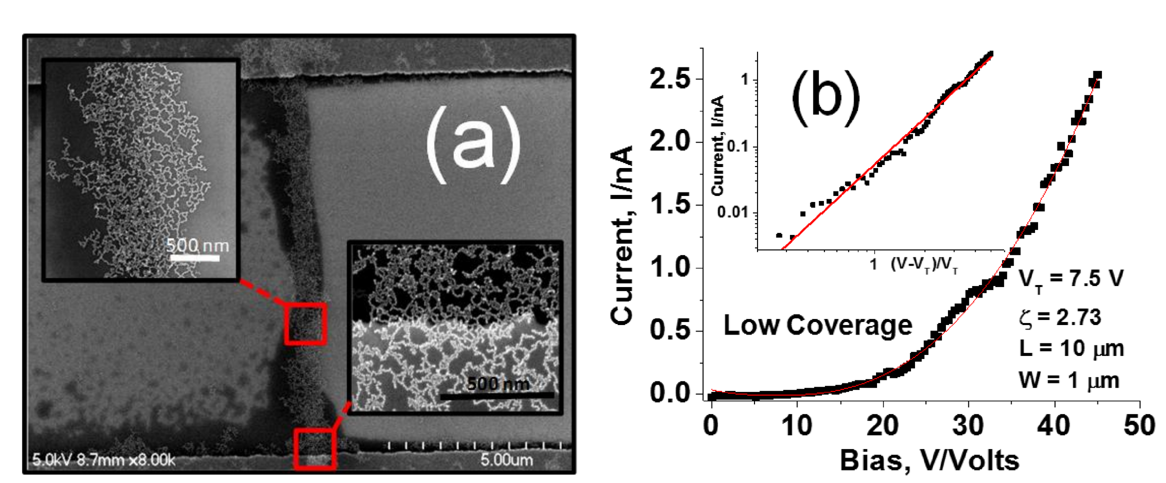
Systematic tuning of the band gap from 0.5 V to 7.5 V at room temperature of a Au nanoparticle's array is shown by controlling the size of the array using soft lithography and electron beam lithography

Methodology

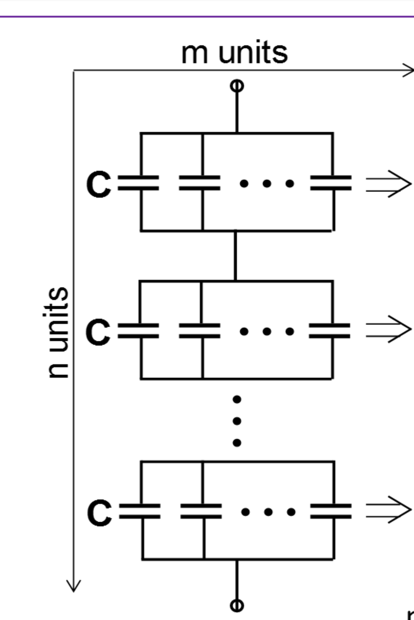
1. Nanoparticle necklaces formation: Cadmium perchlorate solution 3.2mM is added drop-wise to a citrate-functionalized Au nanoparticles 10 nm diameter.
2. A Si chip is prepared by pattern Au electrodes of 50nm thick with different spacing between them from 5µm to 20µm.
3. Bridges of 20µm of PDMS between the gold electrodes are made by soft lithography.
4. The PDMS-patterned chip is activated using an electron beam (3 kV, 10 µA) from a field-emission scanning electron microscope (FESEM, Hitachi S-4700) to form a narrow channel for selective Au necklace deposition. Then the chip is functionalized by NH3 plasma at 80 W and 380 mTorr for 60 seconds.
5. The morphology and dimensions of the selective deposition of Au necklaces were studied by FESEM. Measurement of the electrical properties (I-V behavior) was performed using a home-built system consisting of a high sensitivity Agilent 3458A multimeter and an Agilent 6613C power supply.



Results

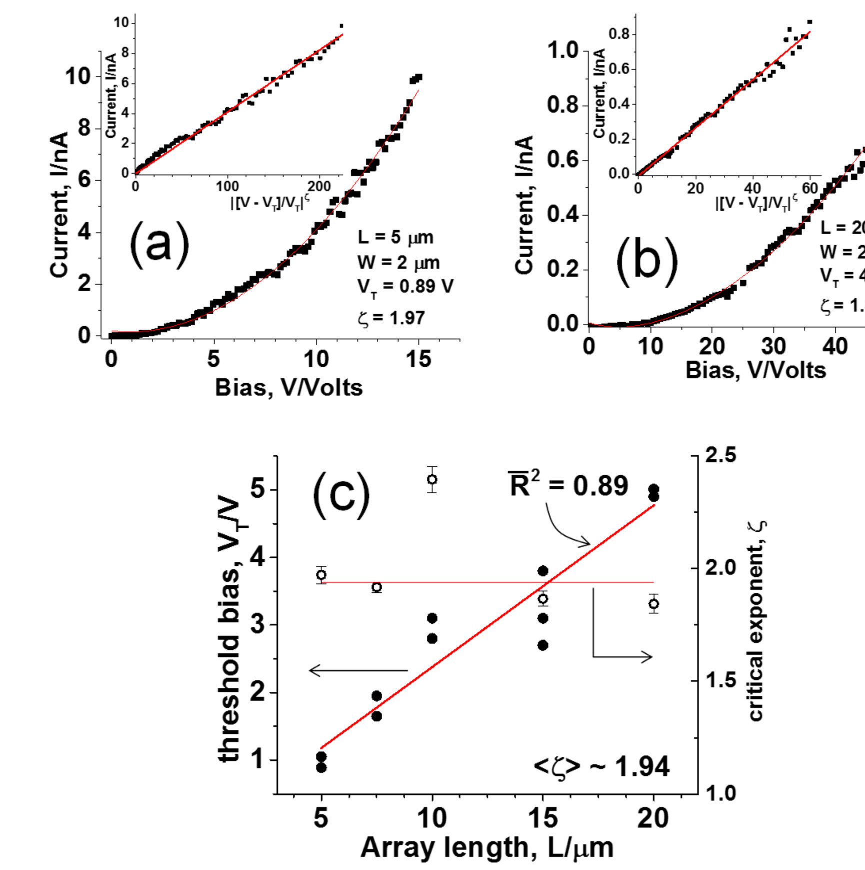


Morphology of Au nanoparticle necklaces and their corresponding electrical behavior. (a) SEM image shows a fabricated device composed of a Au necklace array with a width of ~1 µm and a length of 10 µm. The inset demonstrates good interconnection between the Au necklaces and the Au electrode. (b) Current (I) in response to applied bias (V) for the corresponding necklace network reveals strong Coulomb blockade at room temperature with an exceptionally large V_T of 7.5 V (~300 kT). The inset shows the current as a function of reduced voltage with a critical exponent, ζ of 2.5.

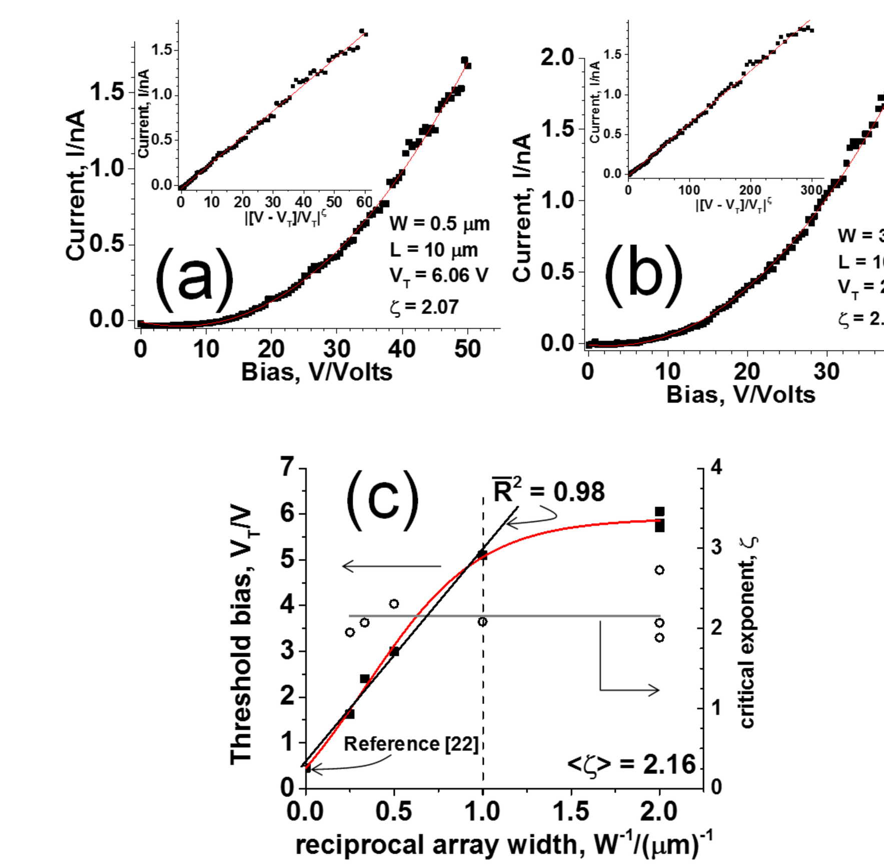


$V_T \sim e/2C_T$
$C_T = mC/n$

Model for necklace network array. The model is composed of capacitors corresponding to single-electron traps. There are m parallel capacitors along the width, and there are n assemblies in series along the length.



Effect of array length on electrical properties at a fixed width of 2µm. (a) and (b) Typical I-V characteristics showing the fit to I ~ $(V - V_T)^ζ$ behavior (inset). (c) V_T is linearly proportional L with a slope of 0.2395; and the average ζ is 1.94.



Effect of array width on electrical properties at a fixed length of 10 µm. (a) and (b) Typical I-V characteristics showing the fit to I ~ $(V - V_T)ζ$ behavior (inset). (c) V_T is linearly proportional W^{-1} (for W ≥ 1 µm) with a slope of 4.624; and the average ζ is 2.16.

Conclusions

- A material for making single-electron devices operating a room temperature with a tunable band gap is presented.
- A tunability of V_T from 0 to 5.5 V (linear) and up to 6 V (nonlinear) was demonstrated by tailoring the size of the array.
- The linear tunability of V_T on array size was explained by a capacitors network model that resulted in the same "normalized" slope for V_T versus L and V_T versus W^{-1}